Mandatory Disclosure

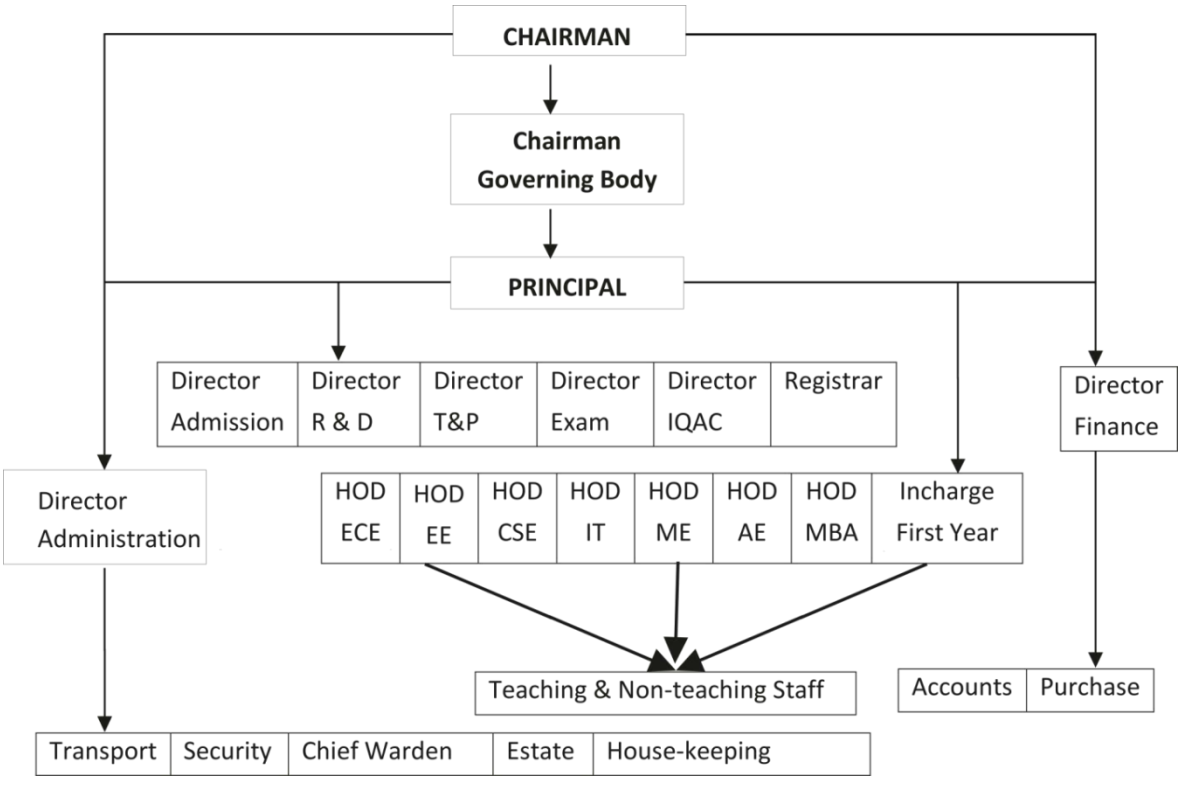
1	Name of the Institution	Vedant College of Engineering And Technology
	Address of the Institution	Vill- Tulsi, Post – Jakhmund, Dist- Bundi
	City & Pin Code	Bundi-323021
	State/UT	Rajasthan
	Longitude & Latitude	75^0 45'9'', 25^0 13'45''
	Phone no. with STD Code	01426-227177
	Fax No. with STD code	01426-227176
	Mobile No.	9414055557
	Email	vcetbundi08@yahoo.com
	Website	www.vedantcollege.org
2	Name of the Organization running the institution	Sanwariya Public School Samiti
	Type of the Organization	Society
	Address of the Organization	Reg. Office : Subhash Nagar, Ajmer Corp. Office: Pal Car Centre Jaipur Road Sikar
	Registered with	Registrar of the societies
	Phone No.	01572-246161
	Mobile	9414037511
	Email	sp.garhwal@gmail.com
3	Name of the Principal/Director	Mr. Satyapal Garhwal
	Designation	Secratery
	Phone no. with STD Code	01572-246161
	Fax No. with STD code	01572-246161
	Mobile	9414037511
	Email	garhwalsp@gmail.com
	Highest Degree	M.Com
	Field of Specialization	Commeres
4	Name of the affiliating University/Board	Board of Technical Education, Rajasthan & Rajasthan Technical University, Kota
	Address	W-6 Residency Road, Jodhpur
	Website	https://techedu.rajasthan.gov.in / rtu.ac.in
	Last Affiliation Period	2024-25

5. Governance

- Members of the Board and their brief background

Sr. No.	Name of Counselor	Designation
1.	Sh. Mool Singh fageria	Chairman
2.	Sh. Ramavtar Meel	Vice Chairman
3.	Mr. Satyapal Garhwal	Secretary
4.	Sh. Chandra Shekhar	Treasurer
5.	Sh. Gopal Singh Garhwal	Member
6.	Sh. Rajveer Singh	Member
7.	Sh. Vijay Kumar Jangid	Member
8.	Sh. Anil Kumar Jhanjadiya	Member
9.	Smt. Mamta	Member
10.	Sh. Anil Kumar	Member
11.	Sh. Shankar Lal Chopra	Member
12.	Sh. Vijaypal	Member
13.	Sh. Nagendra Kumar Tyagi	Member
14.	Sh. Hosiyar Singh	Member
15.	Sh. Deepak Kumar Sharma	Member
16.	Sh. Gopichand Tetarwal	Member

- Organizational chart and processes



- Nature and Extent of involvement of Faculty and students in academic affairs/ improvements
  Faculty practices blended learning, ICT based learning, Innovative Videos, Cut set and Model based learning for improvement of teaching-learning process, Students are encouraged to compete with each other through online quizzes and summarization of e-contents in parallel space with their peer groups, exchange of sample answer and best answers given by the students are discussed among students in which concerned teacher acts as moderator. The TLP system follows blooms taxonomy in design of question paper and content delivery.

- Mechanism/ Norms and Procedure for democratic/ good Governance

  The college follows a transparent mechanism for good governance by practice following

  1. Illustration of evaluated answer scripts to the students.
  2. Committee based various administrative and advisory system in place with fix frequency of meetings and action taken
  3. Well defined Oregano with fix rules and responsibility at each level with vertical and horizontal delegation of roles.
  4. A well defined departmental committees comprising of all internal and external stakeholders with fix frequency of meetings.
  5. A well delegated financial system.
  6. A standard online grievance redressal system supported by various statutory committees

- Student Feedback on Institutional Governance/ Faculty performance
  Students give formal feedback on the prescribed parameters, which reviewed by the top management and the faculty w.r.t. improvement, level up gradation. Informal feedback also taken by the top management from time to time to ensure continuous improvement.

- Grievance Redressal mechanism for Faculty, staff and students
  Grievance redressal mechanism at Vedant College of Engineering & Technology, Bundi underlines accountability and monitoring towards the customers (faculty, staff and students). A se member of committee monitors and addresses the complaints /suggestions received from the stakeholders and appropriate action is taken by the committee. A grievance form has been provided on the college website.

- Establishment of Anti Ragging Committee

Sr. No.	Name of the Committee Member	Position
1	Mr. Inderjeet Sharma	Vice Principal
2	Mr. Shivlal Bairwa	Police Administration
3	Mr. Harvindra Singh Dhilo	SDM Talera
4	Mr. Yogesh Sharma	Faculty Member
5	Mr. Mahesh Sharma	Representative of Student
6	Ms. Madhvi Soni	Representative of Student
7	Mr. Rajesh Nehra	Representative of Non Teaching Staff

- Establishment of Online Grievance Redressal Mechanism : Yes
- Establishment of Grievance Redressal Committee in the Institution and Appointment of OMBUDSMAN by the University

Sr. No.	Name	Position
1	Mr. K.C. Chittora	Coordinator
2	Mr. Jishan Kureshi	Member
3	Mr. Ankur Nagar	Member

- Establishment of Internal Complaint Committee (IC)

Sr.	Name of the Committee Member	Position
1	Ms. Richa	Presiding Officer
2	Mr. K.C. Chittora	Member
3	Mr. Deepak Dadhich	Member

- Establishment of Committee for SC/ ST

Sr. No.	Name	Position
1	Mr. Inderjeet Sharma	CHAIRMAN
2	Ms. Richa	MEMBER
3	MR. Hemant Saini	MEMBER

- **Internal Quality Assurance Cell**

Sr. No.	Name	Position
1	Mr. Inderjeet Sharma	CHAIRMAN
2	Mr. K.C. Chittora	MEMBER
3	MR. Kishan Saini	MEMBER

-

6. Programmes
    - Name of Programmes approved by AICTE

Sr. No.	Name of the Programme	Intake
1	B. Tech. Computer Science and Engineering	30
2	B. Tech. Electronics & Communication Engg	15
3	B. Tech. Electrical Engineering	60
4	B. Tech. Electrical & Electronics Engineering	60
5	B. Tech. Mechanical Engineering	30
6	B. Tech. Civil Engineering	30
7	M. Tech. Computer Science and Engineering	9
8	M. Tech. Power Systems	18
9	Engineering Diploma Civil Engineering	60
10	Engineering Diploma Electrical Engineering	120
11	Engineering Diploma Mechanical Engineering	30

- Programmes Accredited by the NBA – Nil

7.Faculty List

Sr. No.	Name	Designation	Department	Qualification
1	Mr. Inderjeet Sharma	VICE PRINCIPAL	ELECTRONICS & COMMUNICATION ENGG	B.E., M.TECH
2	Dr. A. K. Rathi	PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C., PhD
3	Mr. Kishan Saini	PROFESSOR	ELECTRICAL ENGINEERING	B..TECH
4	Mr. Yogesh Sharma	PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
5	Mr. Murli Suman	PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
6	Mr. Ghanshyam Suman	PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
7	Mr. Jishan Kureshi	PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
8	Ms. Richa Tommar	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.E., M.TECH
9	Mr. Deepak Dadhich	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.
10	Mr. Hemant Saini	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.
11	Mr. Ankur Nagar	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
12	Mr. K.C Chittora	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH,
13	Mr. Arbaz Khan	ASSOCIATE PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C.,
14	Mr. Sunil Jain	ASSOCIATE PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C.,
15	Mr. Vivek Mathur	ASSOCIATE PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C.,
16	Mr. Abhishek Banjara	ASSOCIATE PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C.,
17	Mr. Gajendra Singh	ASSOCIATE PROFESSOR	COMPUTER SCIENCE AND ENGINEERING	B.TECH, M.TECH.
18	Mr. Abhishek Jain	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH, M.TECH
19	Mr. Vishvendra Singh	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.
20	Mr. Prateek Mishra	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
21	Mr.Jitendra Parihar	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
22	Ms. Anjali Vijay	ASSOCIATE PROFESSOR	APPLIED SCIENCE	B.S.C, M.S.C
23	Mr. Ashok Verma	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.

24	Mr. Sarvesh Dayal	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
25	Ms. Neeti Kukhal	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.
26	Mr. Parshant Suman	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
27	Mr. Pankaj Suman	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH.
28	Mr. Harshit Khatri	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
29	Mr. Prem Ranawat	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
30	Mr. Abhimanyu Jaishwal	ASSOCIATE PROFESSOR	MECHANICAL ENGINEERING	B.TECH.
31	Ms. Kriti Sharma	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH, M.TECH
32	Mr. Omprakash Meena	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH, M.TECH
33	Ms. Nidhi Gautam	ASSOCIATE PROFESSOR	CIVIL ENGINEERING	B.TECH, M.TECH
34	Mr.Pushpendra Chandel	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.
35	Mr. Kunal Sharma	ASSOCIATE PROFESSOR	ELECTRICAL ENGINEERING	B.TECH.

8. Fee

- Details of Fee, as approved by State Fee Committee, for the Institution

S.No.	Course	Tuition Fee (Per Annum)	Caution Money (Refundable)
1	B.Tech	Rs. 72000/-	Rs. 7500/-
2	M.Tech	Rs. 72000/-	Rs. 7500/-
3	DIPLOMA	Rs. 30800/-	Rs. 7500/-

- Time schedule for payment of Fee for the entire Programme
    - Semester Wise (At the beginning of each semester)

- Criteria for Fee waivers/scholarship

  Only those candidates who have an annual family income lesser than Rs. 8 Lacs from all possible sources are eligible to apply through the **Fee Waiver** scheme. This seat is allotted to the candidate on the basis of his JEE marks and class XII marks.

- Estimated cost of Boarding and Lodging in Hostels

Sr. No	**Room Type**	**Hostel fee**	**Hostel Security (Refundable)**
1	2-Seater Room	Rs. 80000/-	Rs. 7500/-
2	3-Seater Room	Rs. 70000/-	Rs. 7500/-

9. Admission

Session 2023-24

- No. of Seats Sanctioned

Sr. No.	Name of the Course	Intake
1	B. Tech. Computer Science and Engineering	30
2	B. Tech. Electronics & Communication Engg	15
3	B. Tech. Electrical Engineering	60
4	B. Tech. Electrical & Electronics Engineering	60
5	B. Tech. Mechanical Engineering	30
6	B. Tech. Civil Engineering	30
7	M. Tech. Computer Science and Engineering	9
8	M. Tech. Power Systems	18
9	Engineering Diploma Civil Engineering	60
10	Engineering Diploma Electrical Engineering	120
11	Engineering Diploma Mechanical Engineering	30

- No. of Students Admitted

Sr. No.	Name of the Course	Gen	Min ority	OBC	PH	SC	ST	TFW	Total
1	B. Tech. Computer Science and Engineering	0	0	0	0	0	0	0	0
2	B. Tech. Electronics & Communication Engg	0	0	0	0	0	0	0	0
3	B. Tech. Electrical Engineering	0	0	0	0	0	0	0	0
4	B. Tech. Electrical & Electronics Engineering	0	0	0	0	0	0	0	0
5	B. Tech. Mechanical Engineering	0	0	0	0	0	0	0	0
6	B. Tech. Civil Engineering	0	0	0	0	0	0	0	0
7	M. Tech. Computer Science and Engineering	0	0	0	0	0	0	0	0
8	M. Tech. Power Systems	0	0	0	0	0	0	0	0
9	Engineering Diploma Civil Engineering	5	0	0	0	0	0	0	5
10	Engineering Diploma Electrical Engineering	10	0	0	0	0	0	0	10
11	Engineering Diploma Mechanical Engineering	0	0	0	0	0	0	0	0

Session 2022-23

- No. of Seats Sanctioned

Sr. No.	Name of the Course	Intake
1	B. Tech. Computer Science and Engineering	30
2	B. Tech. Electronics & Communication Engg	15
3	B. Tech. Electrical Engineering	60
4	B. Tech. Electrical & Electronics Engineering	60
5	B. Tech. Mechanical Engineering	30
6	B. Tech. Civil Engineering	30
7	M. Tech. Computer Science and Engineering	9
8	M. Tech. Power Systems	18
9	Engineering Diploma Civil Engineering	60
10	Engineering Diploma Electrical Engineering	120
11	Engineering Diploma Mechanical Engineering	30

- No. of Students Admitted in 2023-24

SR. No.	Name of the Course	Gen	Minority	OBC	PH	SC	ST	TFW	Total Students
1	B. Tech. Computer Science and Engineering	0	0	0	0	0	0	0	0
2	B. Tech. Electronics & Communication Engg	0	0	0	0	0	0	0	0
3	B. Tech. Electrical Engineering	0	0	0	0	0	0	0	0
4	B. Tech. Electrical & Electronics Engineering	0	0	0	0	0	0	0	0
5	B. Tech. Mechanical Engineering	0	0	0	0	0	0	0	0
6	B. Tech. Civil Engineering	0	0	0	0	0	0	0	0
7	M. Tech. Computer Science and Engineering	0	0	0	0	0	0	0	0
8	M. Tech. Power Systems	0	0	0	0	0	0	0	0
9	Engineering Diploma Civil Engineering	16	0	0	0	0	0	0	16
10	Engineering Diploma Electrical Engineering	3	0	0	0	0	0	0	3
11	Engineering Diploma Mechanical Engineering	0	0	0	0	0	0	0	0

11 Admission Procedure for B.Tech Course

- Mention the admission test being followed, name and address of the Test Agency and its URL (website)

  Name of the Test: - JEE (Mains)

  Test Agency: - National Test Agency

  Address: - C-20 1A/8, Sector 62, IITK Outreach Centre, NOIDA-201309

  Website: - nta.ac.in

- Admission Process by:- Rajasthan Engineering Admission Process (REAP)

  Address: - Near Govt. R.C. Khaitan Polytechnic College,
  Jhalana Institutional Area, Jhalana Doongri,
  Jaipur, Rajasthan 302004

  Website: - www.reapraj.com

- Calendar for admission against Management/vacant seats:

  The admission against Management Quota also are done as per the REAP guidelines and schedule. All the details are updated on REAP website time to time.

- Starting of the Academic session : 01st August of Every Year
- The policy of refund of the Fee, in case of withdrawal, shall be clearly notified:

In the event of a student withdrawing before the start of the Course, the entire Fee collected from the student, after a deduction of the processing Fee of not more than Rs. 1000/- (Rupees One Thousand only) shall be refunded by the Institution.

12 Admission Procedure for Engineering Diploma Course

- Admission Process by:- Board of Technical Education Rajasthan Jodhpur

  Address: - W-6 Residency Road, Jodhpur

- Website: - https://techedu.rajasthan.gov.in

- Calendar for admission against Management/vacant seats:

  The admission against Management Quota also are done as per the BTER guidelines and schedule. All the details are updated on BTER website time to time.

- Starting of the Academic session : 01st August of Every Year
- The policy of refund of the Fee, in case of withdrawal, shall be clearly notified:

In the event of a student withdrawing before the start of the Course, the entire Fee collected from the student, after a deduction of the processing Fee of not more than Rs. 1000/- (Rupees One Thousand only) shall be refunded by the Institution.

13 Criteria and Weightages for Admission

- Describe each criterion with its respective weightages i.e. Admission Test, marks in qualifying examination etc.
- Mention the minimum Level of acceptance, if any

  Passed 10+2 examination with Physics/ Mathematics/ Chemistry/ Computer Science/ Electronics/ Information Technology/ Biotechnology/ Informatics Practices/ Biology/ Technical Vocational subject/ Agriculture/ Engineering Graphics/ Business Studies/ Entrepreneurship as per table given below.

  Agriculture Stream (For Agriculture Engineering)

  Obtained at least 45% marks (40% marks in case of candidates belonging to reserved category) in the above subjects taken together.

  OR

  Passed min 3 year Diploma Examination with at least 45% marks (40% marks in case of candidates belonging to reserved category) subject to vacancies in the First Year, in case the vacancies at lateral entry are exhausted

1.3 (a) Diploma/under Graduate Engineering Entry Level qualification 10+2 level

Sr. No.	**Major Disciplines**	**Mandatory Courses at 10+2 Level**	**Other relevant course(s) for this discipline**
1	Aeronautical Engineering	Phy, Chem, Maths	NA
2	Agriculture Engineering**	Phy, Chem OR Agriculture stream	Maths/Biology/Biotechnology/Agriculture/ Agriculture stream
3	Architecture	As per Norms of Council of Architecture (CoA)	
4	Planning	Maths	For remaining two courses select any courses out of 14#
5	Biotechnology**	Phy, Chem	Select any one from Bio/Biotechnology/Maths
6	Ceramic Engineering	Phy, Chem, Maths	NA
7	Civil Engineering	Phy, Chem, Maths	NA
8	Computer Science and Engineering	Phy, Maths	For remaining single course select any courses out of 14#
9	Chemical Engineering	Phy, Chem, Maths	NA
10	Dairy Engineering	Phy, Chem, Maths	NA
11	Electrical Engineering	Phy, Maths	For remaining single course select any courses out of 14#
12	Energy Engineering	Phy, Chem, Maths	NA
13	Electronics Engineering	Phy, Maths	For remaining single course select any courses out of 14#
14	Mechanical Engineering	Phy, Chem, Maths	NA
15	Fire and Safety Engineering	Phy, Chem, Maths	NA
16	Food Engineering	Chem	For remaining two courses select any courses out of 14#

17	Leather Technology	Chem	For remaining two courses select any courses out of 14#
18	Marine Engineering	Phy, Chem, Maths	NA
19	Metallurgy Engineering	Phy, Chem, Maths	NA
20	Military Engineering	Phy, Chem, Maths	NA
21	Mining Engineering	Phy, Chem, Maths	NA
22	Nano Technology	Phy, Chem, Maths	NA
23	Nuclear Science and Technology	Phy, Chem, Maths	NA
24	Packaging Technology	Nil	Select any courses out of 14#
25	Pharmaceutical Engineering**	Phy, Chem	Select any one from Bio/Biotechnology/Maths
26	Printing Engineering	Phy, Chem	For remaining single course select any courses out of 14#
27	Textile Engineering	Phy, Chem, Maths	NA
28	Fashion Technology	Nil	Select any courses out of 14#
29	Textile Chemistry	Chem	For remaining two courses select any courses out of 14#

** First one or two Semesters may be so designed that students with Biology/Biotechnology background have adequate courses on Maths and Vice Versa and then the class is at level studying field for the rest of the semesters.

#Physics/ Mathematics / Chemistry/ Computer Science/Electronics/Information Technology/ Biology/ Informatics Practices/ Biotechnology/ Technical Vocational subject/ Agriculture/ Engineering Graphics/ Business Studies/Entrepreneurship

13. Results of Admission Under Management seats/Vacant seats

- Composition of selection team for admission under Management Quota with the brief profile of members (This information be made available in the public domain after the admission process is over)

  The admission process through qualifying examination and Management Quota are done by REAP office as per their set guidelines and schedule. All the details are updated on REAP website time to time www.reapraj.com

14. Information of Infrastructure and Other Resources Available

- Number of Class Rooms/Tutorial Room/Laboratories/ Drawing Halls/ Computer Centres and size of each

Room No.	**Room Type**	**Area of each room (Sqm.)**
LR-1 to LR-31	Classroom	66
LR-32 & LR-33		33
TR-1- to T-11	Tutorial Room	36
Lab-1, LAB-55	Laboratories	66
WS-1 to WS-5	Workshops	200
SH-1- SH-6	Seminar Hall	140
CC-1 - CC-3	Computer Centre	132

- Central Examination Facility, Number of rooms and capacity of each
  Central Examination Facilities are available in the college having Controller of Examination with his control room and his associated team members. All the lecture halls are used for conduction of college and university level examination. The capacity of each room for examination is around 36 to 48.

- Online Examination Facility (No. of Nodes : - 240, Internet Bandwidth: - 64MBPS)
- Barrier Free Built Environment for disabled and elderly persons
  - All weather approach road inside and outside the campus
  - Availability of lifts in all buildings wherever required
  - Availability of ramps with railings for easy access
  - Specially designed toilets

- Fire and Safety Certificate (Attached as Annexure-4)

- Hostel Facilities

  Separate Hostel facilities for Boys with attached toilets are availablewithin the campus to accommodate 80boys.

  - Library

  Number of Library books/ Titles/ Journals (National/International), E-Library

Sr. No.	**Programme**	**No. of Titles**	**No. of Volumes**	**No. of National Journals**	**E-Journal Subscription**	**E-Library**
1	Engg. & Tech.	4710	23150	69	Yes	Yes (Through DELNET)

  - Laboratory and Workshop (Attached as Annexure-6)

    List of Major Equipment/Facilities in each Laboratory/ Workshop

    List of Experimental Setup in each Laboratory/ Workshop

  - Computing Facilities

    Internet Bandwidth:- 64MBPS

    Number and configuration of System: - 440 (As attached above)

    Total number of system connected by LAN: All

    Total number of system connected by WAN: 01 Main Server

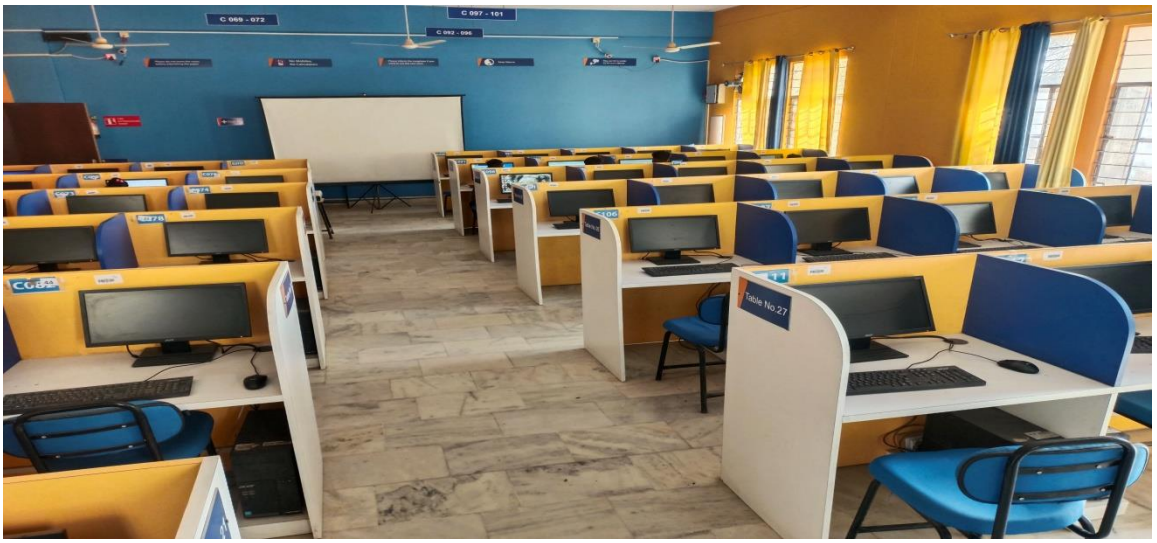
    No. of System Software: - 03

    Major software packages available/Special purpose facilities available

    (Attached as Annexure-7)

- Special Purpose facility available (Conduct of online meetings/webinars/workshops etc.)

- Computer Lab



- List of facilities available

Games and Sports & Cultural

CHESS

Extra-Curricular Activities

(Attached as Annexure-5)

- Soft Skill Development Facilities

The college focuses on the overall development of the students through various soft skill development programs in the respective semesters. The B.Tech 1st year students are taught communication skills in their academic curriculum which focuses on improvement of communication skills and its nuances. Language Lab provides comprehensive practice sessions to the students through ORELL Language Lab Software which comprises of lessons in Phonetics, Group Discussions, Situational Conversations, and Interview Skills etc. The specialized training in the lab prepares the students to be industry ready and also do well in their placements. The B.Tech II year students are taught Technical Communication as a part of their academic curriculum which focuses on professional communication skills pertaining to technical writing and documentation. Soft Skills Training sessions by experts which focus on development of Communication Skills , overall personality enhancement are also conducted to provide an extra edge to the learners and prepare them for future challenges. Soft Skills Workshops and activities like GD, Debates and Extempore competitions are also conducted to motivate the students and exhibit their talent and confidence. The students of 3rd year are also provided focused soft skills training for Interviews, Presentations, and Group Discussions to equip them to face the placements with confidence. Mock interview sessions are conducted to give a real time exposure to the students and they are duly evaluated and informed by the experts to improve their weak areas. Specialized workshops by Industry Experts are also conducted for final year students to provide them exposure to the prevailing trends in the industry. The Reading Club inculcates the habit of reading and comprehending and the newspaper reading activity also improves the awareness and communication skills of the students.

- Teaching Learning Process

  Curricula and syllabus for each of the Programmes as approved by the University

  https://rtu.ac.in/index/view_menudata.php?page=RTU-Syllabus4

  Academic Calendar of the University

  https://rtu.ac.in/index/viewdata.php?page=Academic-Calendar1

  Internal Continuous Evaluation System and place

  (Attached as Annexure-8)

  Student's assessment of Faculty, System in place

  (Attached as Annexure-8)

  Academic Time Table & Teaching load of each faculty

  (Attached as Annexure-9)

For each Post Graduate Courses give the following:

- Title of the Course: - M.Tech. Computer Science and Engineering
- Curricula and Syllabi : -

  https://rtu.ac.in/index/Adminpanel/Images/Media/Computer%20Science%20and%20Engineering.pdf

- Laboratory facilities exclusive to the Post Graduate Course:

  Artificial Intelligence, Privacy and Security
  Researchers in artificial intelligence (AI) seek to understand and develop machines with human-level intelligence by exploring the academic and real-world challenges surrounding AI.

  At Department of Computer Science, we are pioneering breakthroughs in a full spectrum of topics related to AI, including machine learning, computer vision and image processing, human-robot interaction, speech and language analysis, information extraction and privacy protection.

  Our researchers are working in areas where artificial intelligence has been under study for decades—like language—and where the tools are just starting to make inroads—such as efforts to combat human trafficking, diagnose fetal alcohol syndrome, and prevent terrorist attacks using limited resources.

  We understand that the long-term goal of building intelligent machines relies on collaboration across many fields. That's why we also work closely with researchers across application domains, such as health care, social work and linguistics.

  Computer Vision, Robotics and Graphics
  The areas of computer vision, robotics and graphics represent the interface between computers and the rest of the world.

  Robotics at focuses on developing effective, robust, human-centric, and scalable robotic systems. In this area, our expertise ranges from socially assistive robotic and novel haptics technology for virtual touch to complex human-robot interaction and multi-robot systems.

  In computer vision and graphics, our researchers bridge physical and digital worlds with powerful recognition and analysis algorithms, as well as immersive technologies, such as augmented and virtual reality. In computer vision, our strengths include object detection and recognition, face identification, activity recognition, video retrieval and integrating computer vision with natural language queries.

  Our graphics researchers focus on interactive techniques and the simulation and synthesis of multimedia, 3D content and virtual worlds, including image-based modeling and reconstruction, shape analysis, 3D face processing, human digitization, efficient physics simulation, image and video-based rendering techniques

- Title of the Course: - M.Tech. Power Systems
- Curricula and Syllabi : -

  https://rtu.ac.in/index/Adminpanel/Images/Media/Power%20System.pdf
- Laboratory facilities exclusive to the Post Graduate Course:

Sr. No.	Subject name	Subject code	Equipment (No. of PC)	Tool used
1	MATLAB Programming Lab	1MPS5	18	Sci/MAT LAB
2	Power System Modelling & Simulation Lab	2MPS5	18	Sci/MAT LAB

15. MoUs with Industries
    - Shri Sanwariya Stone Suppliers Pvt. Ltd.
    - A-1 Agroseeds Pvt. Ltd.
    - Triputi Balaji Estates Pvt Ltd
    - Ansu Manufacturing Pvt. Ltd.
    - Gradient Softech Pvt Ltd.
16. LoA and subsequent EoA till the current Academic Year

    (Attached as Annexure-10)

17. Accounted audited statement for the last three years

    (Attached as Annexure-11)

18. Best Practices adopted, if any

    (Attached as Annexure-12)

- Fire and Safety Certificate Annexure-4

कार्यालय नगर परिषद,बून्दी

क्रमांकः– 8583 दिनांकः–24/2/20

श्री मुख्य अग्निशमन अधिकारी
नगर निगम, कोटा (राज0)

विषयः– वेदान्त कॉलेज ऑफ इंजि0 एण्ड टेक्नोलोजी महाविद्यालय बून्दी का फायर अनापत्ति पत्र के क्रम में।

महोदय,

उपरोक्त विषयान्तर्गत निवेदन है कि वेदान्त कॉलेज ऑफ इंजि0 एण्ड टेक्नोलोजी महाविद्यालय ग्राम तुलसी,जाखमुण्ड जिला बून्दी द्वारा फायर अनापत्ति प्रमाण पत्र हेतु आवेदन किया गया है और नगर परिषद बून्दी में मुख्य अग्निशमन अधिकारी/ अग्निशमन अधिकारी का पद रिक्त होने से कोटा नगर निगम अग्निशमन अधिकारी द्वारा जारी करने के सम्बन्ध में अपनी राय/अभिशंषा/रिपोर्ट ली जानी है। और पूर्व में भी प्रतिलिपी भेजी जा चुकी हैं।

अतः अनापत्ति प्रमाण पत्र जारी के सम्बन्ध में अपनी रिपोर्ट/अभिशंषा/राय भिजवाने का श्रम करें।

आयुक्त
नगर परिषद,बून्दी

Annexure-6

List of Experimental Setup in each Laboratory/ Workshop

Department of Electronics & Communication Engg

Sr. No.	Name of the Laboratory/Workshop	Experimental Setup available
1.	**Electronic Devices Lab 3EC4-21**	1. Study the following devices: (a) Analog& digital multimeters (b) Function/ Signal generators (c) Regulated d. c. power supplies (constant voltage and constant current operations) (d) Study of analog and digital CRO, measurement of time period, amplitude, frequency & phase angle using Lissajous figures. 2. Plot V-I characteristic of P-N junction diode & calculate cut-in voltage, reverse Saturation current and static & dynamic resistances. 3. Plot the output waveform of half wave rectifier and effect of filters on waveform. Also calculate its ripple factor. 4. Study bridge rectifier and measure the effect of filter network on D.C. voltage output & ripple factor. 5. Plot and verify output waveforms of different clipper and clamper. 6. Plot V-I characteristic of Zener diode 7. Study of Zener diode as voltage regulator. Observe the effect of load changes and determine load limits of the voltage regulator 8. Plot input-output characteristics of BJT in CB, CC and CE configurations. Find their h-parameters. 9. Study of different biasing circuits of BJT amplifier and calculate its Qpoint. 10. Plot frequency response of two stage RC coupled amplifier & calculate its bandwidth. 11. Plot input-output characteristics of field effect transistor and measure Idss and Vp. 12. Plot frequency response curve for FET amplifier and calculate its gain bandwidth product.

2.	**Digital System Design Lab** **3EC4-22**	**Part A: Combinational Circuits** 1. To verify the truth tables of logic gates: AND, OR, NOR, NAND, NOR, Ex-OR and Ex-NOR 2. To verify the truth table of OR, AND, NOR, Ex-OR, Ex-NOR logic gates realized using NAND & NOR gates. 3. To realize an SOP and POS expression. 4. To realize Half adder/ Subtractor& Full Adder/ Subtractor using NAND & NOR gates and to verify their truth tables 5. To design 4-to-1 multiplexer using basic gates and verify the truth table. Also verify the truth table of 8-to-1 multiplexer using IC 6. To design 1-to-4 demultiplexer using basic gates and verify the truth table. Also to construct 1-to-8 demultiplexer using blocks of 1-to-4 demultiplexer **Part B: Sequential Circuits** 7. Using basic logic gates, realize the R-S, J-K and D-flip flops with and without clock signal and verify their truth table. 8. Construct a divide by 2, 4 & 8 asynchronous counter. Construct a 4-bit binary counter for a particular output pattern using D flip flop. 9. Perform input/output operations on parallel in/Parallel out and Serial in/Serial out registers using clock. Also exercise loading only one of multiple values into the register using multiplexer.
3.	**Signal processing Lab** **3EC4-23**	1. Generation of continuous and discrete elementary signals (periodic and non periodic) using mathematical expression. 2. Generation of Continuous and Discrete Unit Step Signal. 3. Generation of Exponential and Ramp signals in Continuous & Discrete domain. 4. Continuous and discrete time Convolution (using basic definition). 5. Adding and subtracting two given signals. (Continuous as well as Discrete signals) 6. To generate uniform random numbers between (0, 1). 7. To generate a random binary wave. 8. To generate and verify random sequences with arbitrary distributions, means and variances for following: (a) Rayleigh distribution (b) Normal distributions: N(0,1). (c) Gaussion distributions: N (m, x) 9. To plot the probability density functions. Find mean and variance for the above distributions
4.	**Computer Programming lab –I** **3EC3-24**	1. Write a simple C program on a 32 bit compiler to understand the concept of array storage, size of a word. The program shall be written illustrating the concept of row major and column major storage. Find the address of element and verify it with the theoretical value. Program may be written for arrays upto 4-dimensions. 2. Simulate a stack, queue, circular queue and dequeue using a

		one dimensional array as storage element. The program should implement the basic addition, deletion and traversal operations. 3. Represent a 2-variable polynomial using array. Use this representation to implement addition of polynomials. 4. Represent a sparse matrix using array. Implement addition and transposition operations using the representation. 5. Implement singly, doubly and circularly connected linked lists illustrating operations like addition at different locations, deletion from specified locations and traversal. 6. Repeat exercises 2, 3 & 4 with linked structures. 7. Implementation of binary tree with operations like addition, deletion, traversal. 8. Depth first and breadth first traversal of graphs represented using adjacency matrix and list. 9. Implementation of binary search in arrays and on linked Binary Search Tree. 10. Implementation of insertion, quick, heap, topological and bubble sorting algorithms.
5.	**Analog and Digital Communication Lab 4EC4-21**	1. Observe the Amplitude modulated wave form & measure modulation index and demodulation of AM signal. 2. Generation & Demodulation of DSB – SC signal. 3. Modulate a sinusoidal signal with high frequency carrier to obtain FM signal and demodulation of the FM signal. 4. Verification of Sampling Theorem. 5. To study & observe the operation of a super heterodyne receiver. 6. PAM, PWM & PPM: Modulation and demodulation. 7. To observe the transmission of four signals over a single channel using TDM-PAM method. 8. To study the PCM modulation & demodulation and study the effect of channel like attenuation, noise in between modulator & demodulator through the experimental setup. 9. To study the Delta & Adaptive delta modulation & demodulation and also study the effect of channel like attenuation, noise in between modulator & demodulator through the experimental setup. 10. To perform the experiment of generation and study the various data formatting schemes (Unipolar, Bipolar, Manchester, AMI etc.) 11. To perform the experiment of generation and detection of ASK, FSK, BPSK, DBPSK signals with variable length data pattern.
6.	**Analog Circuits Lab 4EC4-22**	1. Study and implementation of Voltage Series and Current Series Negative Feedback Amplifier. 2. Study and implementation of Voltage Shunt and Current Shunt Negative Feedback Amplifier.

		3. Plot frequency response of BJT amplifier with and without feedback in the emitter circuit and calculate bandwidth, gain bandwidth product with and without negative feedback. 4. Study and implementation of series and shunt voltage regulators and calculate line regulation and ripple factor. 5. Plot and study the characteristics of small signal amplifier using FET. 6. Study and implementation of push pull amplifier. Measure variation of output power & distortion with load and calculate the efficiency. 7. Study and implementation of Wein bridge oscillator and observe the effect of variation in oscillator frequency. 8. Study and implementation of transistor phase shift oscillator and observe the effect of variation in R & C on oscillator frequency and compare with theoretical value. 9. Study and implementation of the following oscillators and observe the effect of variation of capacitance on oscillator frequency: (a) Hartley (b) Colpitts. 10. Study and implementation of the Inverting And Non-Inverting Operational Amplifier. 11. Study and implementation of Summing, Scaling And Averaging of Operational Amplifier 12. Implementation of active filters using OPAMP.
7.	**Microcontrollers Lab 4EC4-23**	**Following exercises has to be Performed on 8085** 1. Write a program for 1.1 Multiplication of two 8 bit numbers 1.2 Division of two 8 bit numbers 2. Write a program to arrange a set of data in Ascending and Descending order. 3. Write a program to find Factorial of a given number. 4. Write a program to generate a Software Delay. 4.1 Using a Register 4.2 Using a Register Pair **8085 Interfacing Programs** 5. 5.1 Write a program to Interface ADC with 8085. 5.2 Write a program to interface Temperature measurement module with 8085. 6. Write a program to interface Keyboard with 8085. 7. Write a program to interface DC Motor and stepper motor with 8085. Following exercises has to be Performed on 8051 8. Write a program to convert a given Hex number to Decimal. 9. Write a program to find numbers of even numbers and odd numbersamong 10 Numbers. 10. Write a program to find Largest and Smallest Numbers among 10 Numbers. 11. 11.1 To study how to generate delay with timer and loop. 11.2 Write a program to generate a signal on output pin using timer. **8051 Interfacing Programs** 12 12.1 Write a program to interface Seven Segment Display

		with 8051. 12.2 Write a program to interface LCD with 8051. 13 Write a program for Traffic light Control using 8051. 14 Write a program for Elevator Control using 8051.
8.	**Electronics Measurement & Instrumentation Lab 4EC4-24**	1. Measure earth resistance using fall of potential method. 2. Plot V-I characteristics & measure open circuit voltage & short circuit current of a solar panel. 3. Measure unknown inductance capacitance resistance using following bridges (a) Anderson Bridge (b) Maxwell Bridge 4. To measure unknown frequency & capacitance using Wein's bridge. 5. Measurement of the distance with the help of ultrasonic transmitter & receiver. 6. Measurement of displacement with the help of LVDT. 7. Draw the characteristics of the following temperature transducers (a) RTD (Pt-100) (b) Thermistors. 8. Draw the characteristics between temperature & voltage of a K type thermocouple 9. Measurement of strain/force with the help of strain gauge load cell. 10. Study the working of Q-meter and measure Q of coils.
9.	**RF Simulation Lab 5EC4-21**	1 Introduction: Objective, scope and outcome of the course. 2 Study of field pattern of various modes inside a rectangular and circular waveguide. 3 Find the change in characteristics impedance and reflection coefficients of the transmission line by changing the dielectric properties of materials embedded between two conductors. 4 Design and simulate the following Planar Transmission Lines: I. Strip and micro-strip lines II. Parallel coupled strip line III. Coplanar and Slot lines Determine their field patterns and characteristic impedance. 5 Design and simulate the following: I. 3-dB branch line coupler II. Wilkinson power divider III. Hybrid ring IV. Backward wave coupler V. Low pass filters VI. Band pass filters 6 Design RF amplifier using microwave BJT. 7 Design RF amplifier using microwave FET.
10.	**Digital Signal Processing Lab 5EC4-22**	1 Introduction: Objective, scope and outcome of the course. 2 Generation of continuous and discrete elementary signals (impulse,unitstep,ramp) using mathematical expression. 3 Perform basic operations on signals like adding, subtracting, shifting and scaling. 4 Perform continuous and discrete time Convolution (using basic definition). 5 Checking Linearity and Time variance property of a system using convolution, shifting. 6 To generate and verify random sequences with arbitrary distributions, means and variances for following: (a) Rayleigh distribution (b) Normal distributions: N(0,1). (c) Gaussion

		distributions: N (m, x) (d) Random binary wave. 7 To find DFT / IDFT of given DT signal. 8 N-point FFT algorithm. 9 To implement Circular convolution. 10 MATLAB code for implementing z-transform and inverse z-transform. 11 Perform inverse z-transform using residuez MATLAB function. 12 MATLAB program to find frequency response of analog LP/HP filters. 13 To design FIR filter (LP/HP) using windowing (rectangular, triangular, Kaiser) technique using simulink.
11.	**Microwave Lab** **5EC4-23**	1 Introduction: Objective, scope and outcome of the course. 2 Study of various microwave components and instruments like frequency meter, attenuator, detector and VSWR meter. (a) Measurement of guide wavelength and frequency using a X-band slotted line setup. (b) Measurement of low and high VSWR using a X-band slotted line setup. 3 Introduction to Smith chart, measurement of SWR, shift in minimum standing wave with unknown load and calculation of unknown load impedance using Smith chart. 4 Study the behavior of terminated coaxial transmission lines in time and frequency domain. 5 (a) Draw the V-I characteristics of a Gunn diode and determine the output power and frequency as a function of voltage. (b) Study the square wave modulation of microwave signal using PIN diode. 6 Study the square wave modulation of microwave signal using PIN diode.Study and measure the power division and isolation characteristics of a microstrip 3dB power divider. 7 Study of rat race hybrid ring (equivalent of waveguide Magic-Tee) in micro-strip. 8 (a) To study the characteristics of micro-strip 3dB branch line coupler, strip line backward wave coupler as a function of frequency and compare their bandwidth. (b) (b)Measure the microwave input, direct, coupled and isolated powers of a backward wave strip line coupler at the centre frequency using a power meter. From the measurements calculate the coupling, isolation and directivity of the coupler
12.	**Computer Network Lab** **6EC4-21**	1 Introduction: Objective, scope and outcome of the course. 2 PRELIMINARIES: Study and use of common TCP/IP protocols and term viz. telnet rlogin ftp, ping, finger, Socket, Port etc. 3 DATA STRUCTURES USED IN NETWORK PROGRAMMING: Representation of unidirectional, Directional weighted and unweighted graphs. 4 ALGORITHMS IN NETWORKS: computation of shortest

		path for one sourceone destination and one source –all destination 5 hardware realization of the following: i. Encoding schemes: Manchester, NRZ. ii. Error control schemes: CRC, Hamming code.
13.	**Antenna and Wave Propagation Lab 6EC4-22**	**PART-I (Antenna)** 1 Study the gain pattern, HPBW, FNBW and Directivity of a dipole antenna. 2 Measurement of Radiation Pattern, Gain, HPBW of a folded dipole antenna. 3 Measurement of Radiation Pattern, Gain, HPBW of a loop antenna 4 Measurement of Radiation Pattern, Gain, VSWR, input impedance and reflection coefficient for given Monopole antenna 5 Measurement of Radiation Pattern, Gain, VSWR, input impedance and reflection coefficient for given Yagi antennas 6 Study of the Radiation Pattern, Gain, HPBW of a horn antenna 7 Study of the Radiation Pattern, Gain, HPBW of a reflector antennas 8 Study the radiation pattern, gain, VSWR, and input impedance of a rectangular microstrip patch antenna 9 Study the effect of inset feed on the input impedance of a rectangular patch antenna 10 Study the effect of ground plane on the radiation pattern of an antenna 11 Study antenna designing in CST Microwave Studio 12 Design a rectangular microstrip patch antenna using CST MWS **PART-II (Optical Fiber) To perform following experiments based on Fiber Optic Trainer.** 13 To set up Fiber Optic Analog link and Digital link. 14 Measurement of Propagation loss and numerical aperture.
14.	**Electronics Design Lab 6EC4-23**	1 Op-Amp characteristics and get data for input bias current measure the output-offset voltage and reduce it to zero and calculate slew rate. 2 Op-Amp in inverting and non-inverting modes. 3 Op-Amp as scalar, summer and voltage follower. 4 Op-Amp as differentiator and integrator. 5 Design LPF and HPF using Op-Amp 741 6 Design Band Pass and Band reject Active filters using Op-Amp 741. 7 Design Oscillators using Op-Amp (i) RC phase shift (ii) Hartley (iii) Colpitts 8 Design (i) Astable (ii) Monostable multivibrators using IC-555 timer

		9 Design Triangular & square wave generator using 555 timer. 10 Design Amplifier (for given gain) using Bipolar Junction Transistor. 11 Op-Amp characteristics and get data for input bias current measure the output-offsetvoltage and reduce it to zero and calculate slew rate. 12 Op-Amp in inverting and non-inverting modes. 13 Op-Amp as scalar, summer and voltage follower.
15.	**Power Electronics Lab 6EC4-24**	1 Study the characteristics of SCR and observe the terminal configuration, Measure the breakdown voltage, latching and holding current. Plot V-I characteristics. 2 Perform experiment on triggering circuits for SCR. i.e. R triggering, R-C triggering and UJT triggering circuit. 3 Study and test AC voltage regulators using triac, antiparallel thyristors and triac&diac. 4 Study and obtain the waveforms for single-phase bridge converter. 5 Perform experiment on single phase PWM inverter. 6 Perform experiment on buck, boost and buck-boost regulators. 8 Control speed of a single-phase induction motor using single phase AC voltage regulator. 11 Perform experiment on Motor control – open loop & closed loop 12 Design, observe and perform experiment on various type of pulse generation from DSP/ FPGA Platform. Perform experiment for PWM inverters.
16.	**SIGNAL AND IMAGE PROCESSING LAB 7EC7A**	1 To simulate the transmitter and receiver for BPSK 2 To design and simulate FIR digital filter (LP/HP). 3 To design and simulate IIR digital filter (LP/HP). 4 Reading and displaying Gray/ Colour images of different formats 5 RGB/HSI conversions in an image, Image arithmetic operations. 6 Image Histogram and histogram equalization 7 Image filtering in Spatial and frequency domain 8 Morphological operations in analyzing image structures 9 Thresholding-based image segmentation 10 Study of image compression
17.	**WIRELESS COMMUNICATION LAB 7EC8A**	1 Measurement of antenna input characteristics: Measure the input return loss versus frequency in the operating band for (i) Half wave dipole (printed dipole/strip dipole), (ii) Folded dipole and (ii) Log-periodic antenna. 2 Measurement of radiation characteristics of a (i) Half wave dipole (printed dipole/strip dipole), and (ii) Printed Yagi antenna -. Measure radiation patterns in the two principal planes and plot on polar chart. Determine beam width, directivity and antenna

		efficiency. 3 Measurement of antenna gain using absolute gain and relative gain measurements: • Measure gain of Bi-quad antenna using absolute gain measurements. • Measure gain of log-periodic antenna and printed slot antenna using relative gain measurements. 4 Circular polarization measurements on helical antenna. 5 Antenna array theory demonstration using single EM coupled rectangular patch, 2x1 EM coupled and 2x2 EM coupled rectangular patch antennas. 6 Communication link budget calculations- Friis formula and demonstration with transmit and receive antenna setup. 7 Radar Trainer: Working of Doppler radar, velocity of moving object, time and frequency measurement and other applications. 8 To perform Modulation, Demodulation and BER measurement using CDMA – DSSS Trainer. 9 To establish analog/digital communication link and transmit & receive three signals (audio, video, tone) simultaneously using Satellite Communication Trainer. 10 To study GPS Receiver, establishing link between GPS satellite & GPS trainer and measure of latitude & longitude
18.	**RF FABRICATION LAB 8EC5A**	1. Design and fabricate the following Planar Transmission Lines: • Stripline and microstrip lines • Parallel coupled striplines and microstrip lines • Slot lines and Coplanar lines simulate their S-parameters and Characteristic impedance. 2 Design and Fabricate the following; • 3-dB branchline coupler, • backward wave coupler, • Wilkinson power dividers • Low pass filters • band pass filters. simulate their S-parameters & frequency responses.
19.	**VLSI DESIGN & OPTICAL FIBER LAB 8EC7A**	PART-I: Design and simulation of following VLSI circuits using EDA Tools (Software) Schematic design and make Device Level Layout of following circuits. 1. Design 2-input NAND, NOR and XOR using CMOS logic. Obtain its static and dynamic analysis for speed and power dissipation. 2. Design 2X1 and 4X1 Multiplexer using Transmission Gate (TG. Obtain its static and dynamic analysis for speed and power dissipation. 3. Design a SR-latch and D-latch using CMOS. Obtain its static and dynamic analysis for speed and power dissipation. 4. Design a SRAM and DRAM Memory Cell. Obtain its static and dynamic analysis for speed and power dissipation. PART-II Design and simulation of following VLSI circuits using VHDL and then burn/implement the circuits on FPGA kit for real input. 5. Design a 4- bit parallel Adder. Obtain its number of gates, area, and speed and power dissipation.

		6. Design a 4- bit Serial in-serial out shift register. Obtain its number of gates, area, and speed and power dissipation. 7. Design a 4 bit binary synchronous counter. Obtain its number of gates, area, and speed and power dissipation. PART-III. To perform following experiments based on Fiber Optic Trainer. 8. To set up Fiber Optic Analog link. 9. To set up fiber Optic Digital link. 10. Measurement of Propagation loss and numerical aperture. 11. Characterization (VI Characteristics) of laser diode and light emitting diode.

Department of Computer Science and Engineering

S.N.	NAME OF LABORATORY	LIST OF EXPERIMENTS
1	**Cloud Computing Lab**	1. Find procedure to run the virtual machine of different configuration. Check how many virtual machines can be utilized at particular time. 2. Find procedure to attach virtual block to the virtual machine and check whether it holds the data even after the release of the virtual machine. 3. Install a C compiler in the virtual machine and execute a sample program. 4. Show the virtual machine migration based on the certain condition from one node to the other. 5. Find procedure to install storage controller and interact with it. 6. Find procedure to set up the one node Hadoop cluster. 7. Mount the one node Hadoop cluster using FUSE. 8. Write a program to use the API's of Hadoop to interact with it. 9. Write a wordcount program to demonstrate the use of Map and Reduce tasks
2	**Network Programming Lab**	1. Study of Different Type of LAN& Network Equipments.

		2. Study and Verification of standard Network topologies i.e. Star, Bus, Ring etc. 3. LAN installations and Configurations. 4. Write a program to implement various types of error correcting techniques. 5. Write a program to implement various types of framing methods. 6. Write two programs in C: hello_client and hello_server a. The server listens for, and accepts, a single TCP connection; it reads all the data it can from that connection, and prints it to the screen; then it closes the connection b. The client connects to the server, sends the string –Hello, world!‖, then closes the connection 7. Write an Echo_Client and Echo_server using TCP to estimate the round trip time from client to the server. The server should be such that it can accept multiple connections at any given time. 8. Repeat Exercises 6 & 7 for UDP. 9. Repeat Exercise 7 with multiplexed I/O operations. 10. Simulate Bellman-Ford Routing algorithm in NS2.
3	**Linux Shell Programming Lab**	1. Use of Basic Unix Shell Commands: ls, mkdir, rmdir, cd, cat, banner, touch, file, wc, sort, cut, grep, dd, dfspace, du, ulimit. 2. Commands related to inode, I/O redirection and piping, process control commands, mails. 3. Shell Programming: Shell script based on control structure- If-then-fi, if-thenelse-if, nested if-else, to find: 3.1 Greatest among three numbers. To find a year is leap year or not. To input angles of a triangle and find out whether it is valid triangle or not. To check whether a character is alphabet, digit or

		special character. 3.5 To calculate profit or loss. 4. Shell Programming - Looping- while, until, for loops 4.1 Write a shell script to print all even and odd number from 1 to 10. 4.2 Write a shell script to print table of a given number 4.3 Write a shell script to calculate factorial of a given number. Write a shell script to print sum of all even numbersfrom 1 to 10. Write a shell script to print sum of digit of any number.5. Shell Programming - case structure, use of break 5.1 Write a shell script to make a basic calculator which performs addition, subtraction, Multiplication, division 5.2 Write a shell script to print days of a week. 5.3 Write a shell script to print starting 4 months having 31 days. 6. Shell Programming - Functions Write a shell script to find a number is Armstrong ornot. Write a shell script to find a number is palindrome ornot. Write a shell script to print Fibonacci series.6.4 Write a shell script to find prime number. 6.5 Write a shell script to convert binary to decimal and decimal to binary 7. Write a shell script to print different shapes- Diamond, triangle, square, rectangle, hollow square etc. 8. Shell Programming – Arrays Write a C program to read and print elements of array. Write a C program to find sum of all array elements.8.3 Write a C program to find reverse of an array.

		Write a C program to search an element in an array. Write a C program to sort array elements in ascendingor descending order
4	**Database Management System Lab**	1. Design a Database and create required tables. For e.g. Bank, College Database 2. Apply the constraints like Primary Key, Foreign key, NOT NULL to the tables. 3. Write a SQL statement for implementing ALTER,UPDATE and DELETE. 4. Write the queries to implement the joins. 5. Write the query for implementing the following functions: MAX (), MIN (), AVG () and COUNT (). 6. Write the query to implement the concept of Integrity constrains. 7. Write the query to create the views. 8. Perform the queries for triggers. 9. Perform the following operation for demonstrating the insertion , updation and deletion 10.Using the referential integrity constraints. 11.Write the query for creating the users and their role.
5	**Python Lab**	**List of Experiments** 1 Write a program to demonstrate basic data type in python. 2 Write a program to compute distance between two points taking input from the user Write a program add.py that takes 2 numbers as command line arguments and prints its sum. 3 Write a Program for checking whether the given number is an even number or not. Using a for loop, write a program that prints out the decimal equivalents of 1/2, 1/3, 1/4, . . . , 1/10 4 Write a Program to demonstrate list and tuple in python.

		Write a program using a for loop that loops over a sequence. Write a program using a while loop that asks the user for a number, and prints a countdown from that number to zero. 5 Find the sum of all the primes below two million. By considering the terms in the Fibonacci sequence whose values do not exceed four million, WAP to find the sum of the even-valued terms. 6 Write a program to count the numbers of characters in the string and store them in a dictionary data structure Write a program to use split and join methods in the string and trace a birthday of a person with a dictionary data structure 7 Write a program to count frequency of characters in a given file. Can you use character frequency to tell whether the given file is a Python program file, C program file or a text file? Write a program to count frequency of characters in a given file. Can you use character frequency to tell whether the given file is a Python program file, C program file or a text file? 8 Write a program to print each line of a file in reverse order. Write a program to compute the number of characters, words and lines in a file. 9 Write a function nearly equal to test whether two strings are nearly equal. Two strings a and b are nearly equal when a can be generated by a single mutation on. Write function to compute gcd, lcm of two numbers. Each function shouldn't exceed one line. 10 Write a program to implement Merge sort. Write a pgm to implement Selection sort, Insertion sort.

6	**Machine Learning Lab**	1 Implement and demonstrate the FIND-S algorithm for finding the most specific hypothesis based on a given set of training data samples. Read the training data from a .CSV file. 2 For a given set of training data examples stored in a .CSV file, implement and demonstrate the Candidate-Elimination algorithm to output a description of the set of all hypotheses consistent with the training examples. 3 Write a program to demonstrate the working of the decision tree based ID algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample 4 Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets 5 Write a program to implement the naïve Bayesian classifier for a sample training data set stored as a .CSV file. Compute the accuracy of the classifier, considering few test data sets. 6 Assuming a set of documents that need to be classified, use the naïve Bayesian Classifier model to perform this task. Built-in Java classes/API can be used to write the program. Calculate the accuracy, precision, and recall for your data set. 7 Write a program to construct a Bayesian network considering medical data. Use this model to demonstrate the diagnosis of heart patients using standard Heart Disease Data Set. You can use Java/Python ML library classes/API. 8 Apply EM algorithm to cluster a set of data stored in a .CSV file. Use the same data set for clustering using k-Means algorithm. Compare the results of these two algorithms and comment on the quality of clustering. You can add Java/Python ML library classes/API in the program. 9 Write a program to implement k-Nearest Neighbour algorithm to classify the iris data set. Print both correct and wrong predictions. Java/Python ML library classes can be used for this problem. 10 Implement the non-parametric Locally Weighted Regression algorithm in order to fit data points. Select appropriate data set for your experiment and draw graphs.
7	**Mobile Application Development Lab**	1 To study Android Studio and android studio installation. Create ‒Hello World‖ application. 2 To understand Activity, Intent, Create sample application with login module.(Check username and password). 3 Design simple GUI application with activity and intents e.g. calculator.

		4 Develop an application that makes use of RSS Feed. 5 Write an application that draws basic graphical primitives on the screen 6 Create an android app for database creation using SQLite Database. 7 Develop a native application that uses GPS location information 8 Implement an application that writes data to the SD card. 9 Design a gaming application 10 Create an application to handle images and videos according to size.
8	**Java Lab**	1. Develop an in depth understanding of programming in Java: data types, variables, operators, operator precedence, Decision and control statements, arrays, switch statement, Iteration Statements, Jump Statements, Using break, Using continue, return. 2. Write Object Oriented programs in Java: Objects, Classes constructors, returning and passing objects as parameter, Inheritance, Access Control, Using super, final with inheritance Overloading and overriding methods, Abstract classes, Extended classes. 3. Develop understanding to developing packages & Interfaces in Java: Package, concept of CLASSPATH, access modifiers, importing package, Defining and implementing interfaces. 4. Develop understanding to developing Strings and exception handling: String constructors, special string operations, character extraction, searching and comparing strings, string Buffer class. Exception handling fundamentals, Exception types, uncaught exceptions, try, catch and multiple catch statements. Usage of throw, throws and finally. 5. Develop applications involving file handling: I/O streams, File I/O. 6. Develop applications involving concurrency: Processes and Threads, Thread Objects, Defining and Starting a Thread, Pausing Execution with Sleep, Interrupts, Joins, and Synchronization. **Indicative List of exercises:** 7. Programs to demonstrate basic concepts e.g. operators, classes, constructors, control & iteration statements, recursion etc. such as complex arithmetic, matrix arithmetic, tower of Hanoi problem etc. 8. Development of programs/projects to demonstrate concepts like inheritance, exception handling, packages, interfaces etc. such as application for electricity department, library management, ticket reservation system, payroll system etc.

		9. Development of a project to demonstrate various file handling concepts. 10. Develop applications involving Applet: Applet Fundamentals, using paint method and drawing polygons. It is expected that each laboratory assignments to given to the students with an aim to In order to achieve the above objectives.
9	**UNIX SHELL PROGRAMMING**	1. Use of Basic Unix Shell Commands: ls, mkdir, rmdir, cd, cat, banner, touch, file, wc, sort, cut, grep, dd, dfspace, du, ulimit. 2. Commands related to inode, I/O redirection and piping, process control commands, mails. 3. Shell Programming: Shell script exercises based on following (i) Interactive shell scripts (ii) Positional parameters (iii) Arithmetic (iv) if-then-fi, if-then-else-fi, nested if-else (v) Logical operators (vi) else + if equals elif, case structure (vii) while, until, for loops, use of break (viii) Metacharacters (ix) System administration: disk management and daily administration 4. Write a shell script to create a file in $USER class/batch directory. Follow the instructions (i) Input a page profile to yourself, copy it into other existing file; (ii) Start printing file at certain line (iii) Print all the difference between two file, copy the two files at $USER/CSC/2007 directory. (iv) Print lines matching certain word pattern. 5. Write shell script for- (i) Showing the count of users logged in, (ii) Printing Column list of files in your home directory (iii) Listing your job with below normal priority (iv) Continue running your job after logging out. 6. Write a shell script to change data format .Show the time taken in execution of this script 7. Write a shell script to print files names in a directory showing date of creation & serial number of the file. 8. Write a shell script to count lines, words and characters in its input(do not use wc). 9. Write a shell script to print end of a Glossary file in reverse order using Array. (Use awk tail) 10. Write a shell script to check whether Ram logged in, Continue checking further after every 30 sec till success.

10	**Digital Image Processing Lab**	1 Point-to-point transformation. This laboratory experiment provides for thresholding an image and the evaluation of its histogram. Histogram equalization. This experiment illustrates the relationship among the intensities (gray levels) of an image and its histogram. 2 Geometric transformations. This experiment shows image rotation, scaling, and translation. Two-dimensional Fourier transform 3 Linear filtering using convolutions. Highly selective filters. 4 Ideal filters in the frequency domain. Non Linear filtering using convolutional masks. Edge detection. This experiment enables students to understand the concept of edge detectors and their operation in noisy images. 5 Morphological operations: This experiment is intended so students can appreciate the effect of morphological operations using a small structuring element on simple binary images. The operations that can be performed are erosion, dilation, opening, closing, open-close, close-open. 1 Color image segmentation algorithm development 2 Wavelet/vector quantization compression 3 Deformable templates applied to skin tumor border finding 4 Helicopter image enhancement 5 High-speed film image enhancement 6 Computer vision for skin tumor image evaluation 7 New Border Images
11	**FPGA LAB.**	1.Fundamental Theory Introduction to DSP architectures and programming Sampling Theory, Analog-to-Digital Converter (ADC), Digital-to Analog Converter (DAC), and Quantization; Decimation, Interpolation, Convolution, Simple Moving Average; Periodic Signals and harmonics; Fourier Transform (DFT/FFT), Spectral Analysis, and time/spectrum representations; FIR and IIR Filters; 2. Design (Simulation) using MATLAB/ Simulink Simulate the lab exercises using MATLAB/Simulink 3. Implementation using pure DSP, pure FPGA and Hybrid DSP/FPGA platforms Digital Communications: On-Off-Keying (OOK), BPSK modulation, and a simple transceiver design Adaptive Filtering: Echo/Noise Cancellation, Least Mean Square (LMS) algorithm (2 weeks) Wireless Communications: Channel coding/decoding, Equalization, Simple Detection Algorithm, OFDM Speech Processing: Prediction Algorithms, Speech Classification and Synthesis

12	**Data Structures and Algorithms Lab**	1.Write a simple C program on a 32 bit compiler to understand the concept of array storage, size of a word. The program shall be written illustrating the concept of row major and column major storage. Find the address of element and verify it with the theoretical value. Program may be written for arrays up to 4-dimensions. 2 Simulate a stack, queue, circular queue and dequeue using a one dimensional array as storage element. The program should implement the basic addition, deletion and traversal operations. 3 Represent a 2-variable polynomial using array. Use this representation to implement addition of polynomials 4 Represent a sparse matrix using array. Implement addition and transposition operations using the representation. 5 Implement singly, doubly and circularly connected linked lists illustrating operations like addition at different locations, deletion from specified locations and traversal. 6 Repeat exercises 2, 3 & 4 with linked structure. 7 Implementation of binary tree with operations like addition, deletion, traversal. 8 Depth first and breadth first traversal of graphs represented using adjacency matrix and list. 9 Implementation of binary search in arrays and on linked Binary Search Tree. 10 Implementation of different sorting algorithm like insertion, quick, heap, bubble and many more sorting algorithms.
13	**Object Oriented Programming Lab**	1 Understand the basics of C++ library, variables, data input-output. 2 C++ program using with the concept of structures. 3 Implement class and object concepts and function overloading. 4 Write programs to understand dynamic memory allocation and array of objects. 5 Program to understand different types of constructors and destructor. 6 Implement friend function to access private data of a class and usage of this pointer. 7 Write programs to understand the usage of constant data member and member function, static data member and member function in a class. 8 Implement different types of inheritance, function overriding and virtual function 9 Implement Operator overloading concepts. 10 Write programs to understand function template and

		class template. 11 Write programs to understand exception handling techniques. 12 Write programs to understand file handling techniques.
14	**Software Engineering Lab**	1. Development of requirements specification, function oriented design using SA/SD, object-oriented design using UML, test case design, implementation using Java and testing. Use of appropriate CASE tools and other tools such as configuration management tools, program analysis tools in the software life cycle. 2 Develop Software Requirements Specification (SRS) for a given problem in IEEE template. 3 Develop DFD model (level-0, level-1 DFD and Data dictionary) of the project. 4 Develop structured design for the DFD model developed. 5 Developed all Structure UML diagram of the given project. 6 Develop Behavior UML diagram of the given project. 7 Manage file, using ProjectLibre project management software tool.
15	**Digital Electronics Lab**	1 To verify the truth tables of basic logic gates: AND, OR, NOR, NAND, NOR. Also to verify truth table of Ex-OR, Ex-NOR (For 2, 3, & 4 inputs using gateswith 2, 3, & 4 inputs). 2 To verify the truth table of OR, AND, NOR, Ex-OR, Ex-NOR realized usingNAND& NOR gates. 3 To realize an SOP and POS expression. 4 To realize Half adder/ Subtractor& Full Adder/ Subtractor using NAND & NOR gatesand to verify their truth tables. 5 To realize a 4-bit ripple adder/ Subtractor using basic Half adder/ Subtractor& basic Full Adder/ Subtractor. 6 To verify the truth table of 4-to-1 multiplexer and 1-to-4 demultiplexer. Realize the multiplexer using basic gates only. Also to construct and 8-to-1 multiplexer and 1-to-8 demultiplexer using blocks of 4-to-1 multiplexer and 1-to-4 demultiplexer. 7 Design & Realize a combinational circuit that will accept a 2421 BCD code and drive a TIL -312 seven-segment display. 8 Using basic logic gates, realize the R-S, J-K and D-flip flops with and without clock signal and verify their truth table. 9 Construct a divide by 2,4& 8 asynchronous counter. Construct a 4-bit binary counter and ring counter for a particular output pattern using D flip flop. 10 Perform input/output operations on parallel in/Parallel out and Serial in/Serial out registers using clock. Also

		exercise loading only one of multiple values into the register using multiplexer. Note: As far as possible, the experiments shall be performed on bread board. However, experiment Nos. 1-4 are to be performed on bread board only.
16	**Computer Graphics & Multimedia Lab**	1 Implementation of Line, Circle and ellipse attributes 2 To plot a point (pixel) on the screen 3 To draw a straight line using DDA Algorithm 4 Implementation of mid-point circle generating Algorithm 5 Implementation of ellipse generating Algorithm 6 Two Dimensional transformations - Translation, Rotation, Scaling, Reflection, Shear 7 Composite 2D Transformations 8 Cohen Sutherland 2D line clipping and Windowing 9 Sutherland – Hodgeman Polygon clipping Algorithm 10 Three dimensional transformations - Translation, Rotation, Scaling 11 Composite 3D transformations 12 Drawing three dimensional objects and Scenes 13 Generating Fractal images
17	**Compiler Design Lab**	1 Introduction: Objective, scope and outcome of the course. 2 To identify whether given string is keyword or not. 3 Count total no. of keywords in a file. [Taking file from user] 4 Count total no of operators in a file. [Taking file from user] 5 Count total occurrence of each character in a given file. [Taking file from user] 6 Write a C program to insert, delete and display the entries in Symbol Table. 7 Write a LEX program to identify following: 1. Valid mobile number 2. Valid url 3. Valid identifier 4. Valid date (dd/mm/yyyy) 5. Valid time (hh:mm:ss) 8 Write a lex program to count blank spaces,words,lines in a given file. 9 Write a lex program to count the no. of vowels and consonants in a C file. 10 Write a YACC program to recognize strings aaab,abbb using a^nb^n, where b>=0. 11 Write a YACC program to evaluate an arithmetic expression involving operators +,-,* and /. 12 Write a YACC program to check validity of a strings abcd,aabbcd using grammar a^nb^nc^md^m, where n , m>0 13 Write a C program to find first of any grammar.

18	**Analysis of Algorithms Lab**	1 Sort a given set of elements using the Quicksort method and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n. The elements can be read from a file or can be generated using the random number generator. 2 Implement a parallelized Merge Sort algorithm to sort a given set of elements and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n. The elements can be read from a file or can be generated using the random number generator. 3 a. Obtain the Topological ordering of vertices in a given digraph. b. Compute the transitive closure of a given directed graph using Warshall's algorithm. 4 Implement 0/1 Knapsack problem using Dynamic Programming. 5 From a given vertex in a weighted connected graph, find shortest paths to other vertices using Dijkstra's algorithm. 6 Find Minimum Cost Spanning Tree of a given undirected graph using Kruskal's algorithm. 7 a. Print all the nodes reachable from a given starting node in a digraph using BFS method. b. Check whether a given graph is connected or not using DFS method. 8. Find Minimum Cost Spanning Tree of a given undirected graph using Prim's algorithm. 9. Implement All-Pairs Shortest Paths Problem using Floyd's algorithm. 10 Implement N Queen's problem using Back Tracking.
19	**Advance Java Lab**	1 Introduction To Swing, MVC Architecture, Applets, Applications and Pluggable Look and Feel, Basic swing components : Text Fields, Buttons, Toggle Buttons, Checkboxes, and Radio Buttons 2 Java database Programming, java.sql Package, JDBC driver, Network Programming With java.net Package, Client and Server Programs, Content And Protocol Handlers 3 RMI architecture, RMI registry, Writing distributed application with RMI, Naming services, Naming And Directory Services, Overview of JNDI, Object serialization and Internationalization 4 J2EE architecture, Enterprise application concepts, n-tier application concepts, J2EE platform, HTTP protocol, web application, Web containers and Application servers 5 Server side programming with Java Servlet, HTTP and Servlet, Servlet API, life cycle, configuration and context,

		Request and Response objects, Session handling and event handling, Introduction to filters with writing simple filter application 6 JSP architecture, JSP page life cycle, JSP elements, Expression Language, Tag Extensions, Tag Extension API, Tag handlers, JSP Fragments, Tag Files, JSTL, Core Tag library, overview of XML Tag library, SQL Tag library and Functions Tag library.
20	**Web Development Lab**	1 . Creation of HTML Files 2 Working with Client Side Scripting : VBScript, JavaScript 3 Configuration of web servers: Apache Web Server, Internet Information Server (IIS) 4 Working with ActiveX Controls in web documents 5 Experiments in Java Server Pages: Implementing MVC Architecture using Servlets, Data Access Programming (using ADO), Session and Application objects, File System Management 6 Working with other Server Side Scripting: Active Server Pages, Java Servlets, PHP 7 Experiments in Ajax Programming 8 Developing Web Services 9 Developing any E-commerce application (Mini Project) 10 Application Development in cloud computing Environment 11 Experiment Using Open Source Tool e.g. ANEKA
21	**VLSI PHYSICAL DESIGN LAB**	VLSI Physical Design Automation is essentially the research, development and productization of algorithms and data structures related to the physical design process. The objective is to investigate optimal arrangements of devices on a plane (or in three dimensions) and efficient interconnection schemes between these devices to obtain the desired functionality and performance. Since space on a wafer is very expensive real estate, algorithms must use the space very efficiently to lower costs and improve yield. In addition, the arrangement of devices plays a key role in determining the performance of a chip. Algorithms for physical design must also ensure that the layout generated abides by all the rules required by the fabrication process. Fabrication rules establish the tolerance limits of the fabrication process. Finally, algorithms must be efficient and should be able to handle very large designs. Efficient algorithms not only lead to fast turn-around time, but also permit designers to make iterative improvements to the layouts. The VLSI physical design process manipulates very simple geometric objects, such as polygons and lines. As a result, physical design algorithms tend to be very intuitive in nature, and have significant overlap with graph

		algorithms and combinatorial optimization algorithms. In view of this observation, many consider physical design automation the study of graph theoretic and combinatorial algorithms for manipulation of geometric objects in two and three dimensions. However, a pure geometric point of view ignores the electrical (both digital and analog) aspect of the physical design problem. In a VLSI circuit, polygons and lines have inter-related electrical properties, which exhibit a very complex behavior and depend on a host of variables. Therefore, it is necessary to keep the electrical aspects of the geometric objects in perspective while developing algorithms for VLSI physical design automation. With the introduction of Very Deep Sub-Micron (VDSM), which provides very small features and allows dramatic increases in the clock frequency, the effect of electrical parameters on physical design will play a more dominant role in the design and development of new algorithms. The exercise should be such that the above objectives are met. Automation tools such as Synopsis/ Cadence are available in the area. However, to begin, the students shall be assigned exercises on route optimization, placement & floor planning. Small circuits may be taken & algorithms implemented. At a later stage, the students may use tools and design more complex circuits.
22	**COMPILER DESIGN LAB**	Objectives: At the end of the semester, the students should have clearly understood and implemented the following: 1. Develop an in depth understanding of system programming concept. Lexical analysis, syntax analysis, semantics analysis, code optimization, code generation. Language specification and processing 2. Develop an Understanding of Scanning by using concept of Finite state automaton. Parse tree and syntax tree, Top down parsing (recursive decent parsing, LL (1) parser) Bottom up parsing (operator precedence parsing) .Managing symbol table, opcode table, literal table, pool table 3. Develop an Understanding of Intermediate code form: Three address code, Polish notation (Postfix strings) 4. Develop an Understanding of Allocation data structure. Heaps 5. Develop an Understanding about Language processor development tools: LEX, YACC. Language processing activities (Program generation and execution It is expected that each laboratory assignments to given to the students with an aim to In order to achieve the above objectives Indicative List of exercises: 1. Write grammar for a fictitious language and create a

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		lexical analyzer for the same. 2. Develop a lexical analyzer to recognize a few patterns in PASCAL and C (ex: identifiers, constants, comments, operators etc.) 3. Write a program to parse using Brute force technique of Top down parsing 4. Develop on LL (1) parser (Construct parse table also). 5. Develop an operator precedence parser (Construct parse table also) 6. Develop a recursive descent parser 7. Write a program for generating for various intermediate code forms i) Three address code ii) Polish notation 8. Write a program to simulate Heap storage allocation strategy 9. Generate Lexical analyzer using LEX 10. Generate YACC specification for a few syntactic categories 11. Given any intermediate code form implement code optimization techniques
23	**Research Lab (M.Tech)**	**Artificial Intelligence, Privacy and Security** Researchers in artificial intelligence (AI) seek to understand and develop machines with human-level intelligence by exploring the academic and real-world challenges surrounding AI. At Department of Computer Science, we are pioneering breakthroughs in a full spectrum of topics related to AI, including machine learning, computer vision and image processing, human-robot interaction, speech and language analysis, information extraction and privacy-protection. Our researchers are working in areas where artificial intelligence has been under study for decades—like language—and where the tools are just starting to make inroads—such as efforts to combat human trafficking, diagnose fetal alcohol syndrome, and prevent terrorist attacks using limited resources. We understand that the long-term goal of building intelligent machines relies on collaboration across many fields. That's why we also work closely with researchers across application domains, such as health care, social work and linguistics. **Computer Vision, Robotics and Graphics** The areas of computer vision, robotics and graphics represent the interface between computers and the rest of the world. Robotics at arfocuses on developing effective, robust, human-centric, and scalable robotic systems. In this area, our expertise ranges from socially assistive robotic and novel haptics technology for virtual touch to complex

		human-robot interaction and multi-robot systems. In computer vision and graphics, our researchers bridge physical and digital worlds with powerful recognition and analysis algorithms, as well as immersive technologies, such as augmented and virtual reality. In computer vision, our strengths include object detection and recognition, face identification, activity recognition, video retrieval and integrating computer vision with natural language queries. Our graphics researchers focus on interactive techniques and the simulation and synthesis of multimedia, 3D content and virtual worlds, including image-based modeling and reconstruction, shape analysis, 3D face processing, human digitization, efficient physics simulation, image and video-based rendering techniques

Department of Electrical Engineering

S.NO.	NAME OF LABORATORY/ WORKSHOP	EXPERIMENTAL SETUP AVAILABLE
1.	ANALOG ELECTRONICS LAB	1. Plot gain-frequency characteristics of BJT amplifier with and without negative feedback in the emitter circuit and determine bandwidths, gain bandwidth products and gains at 1 kHz with and without negative feedback. 2. Study of series and shunt voltage regulators and measurement of line and load regulation and ripple factor. 3. Plot and study the characteristics of small signal amplifier using FET. 4. Study of push pull amplifier. Measure variation of output power & distortion with load. 5. Study Wein bridge oscillator and observe the effect of variation in R & C on oscillator frequency 6. Study transistor phase shift oscillator and observe the effect of variation in R & C on oscillator frequency and compare with theoretical value. 7. Study the following oscillators and observe the effect of variation of C on oscillator frequency: (a) Hartley (b) Colpitts. 8. To plot the characteristics of UJT and UJT as relaxation.

2.	ELECTRICAL MACHINE-I LAB	1. To perform O.C. and S.C. test on a 1-phase transformer and to determinethe parameters of its equivalent circuit its voltage regulation and efficiency. 2. To perform sumpner's test on two identical 1-phase transformers and findtheir efficiency & parameters of the equivalent circuit. 3. To determine the efficiency and voltage regulation of a single-phasetransformer by direct loading. 4. To perform the heat run test on a delta/delta connected 3-phasetransformer and determine the parameters for its equivalent circuit. 5. To perform the parallel operation of the transformer to obtain data to study the load sharing. 6. Separation of no load losses in single phase transformer. 7. To study conversion of three-phase supply to two-phase supply using Scott-Connection. 8. Speed control of D.C. shunt motor by field current control method & plot thecurve for speed verses field current. 9. Speed control of D.C. shunt motor by armature voltage control method &plot the curve for speed verses armature voltage. 10. To determine the efficiency at full load of a D.C shunt machine consideringit as a motor by performing Swinburne's test. 11. To perform Hopkinson's test on two similar DC shunt machines and henceobtain their efficiencies at various loads.
3.	ELECTRICAL CIRCUIT DESIGN LAB	1. Introduction to Datasheet Reading. 2. Introduction to Soldering - Desoldering process and tools. 3. Simulate characteristic of BJT and UJT. Validate on Bread Board orPCB. 4. Simulate Bridge Rectifier Circuit and validate on Bread Board or PCB.a) Half Bridge.b) Full Bridge. 5. Simulate Regulated Power Supply and validate on Bread Board or PCB. a) Positive Regulation (03 Volt to 15 Volt).

		b) Negative Regulation (03 Volt to 15 Volt). c) 25 Volt, 1–10 A Power Supply. 6. Simulate Multivibrator circuit using IC 555 and BJT separately. Validateon Bread Board or PCB.a) Astable Mode.b) Bistable Mode.c) Monostable Mode. 7. Introduction to Sensors to measure real time quantities and theirimplementation in different processes.(Proximity, Accelerometer, Pressure, Photo-detector, UltrasonicTransducer, Smoke, Temperature, IR, Color, Humidity, etc.). 8. Hardware implementation of temperature control circuit usingThermistor. 9. Simulate Frequency divider circuit and validate it on Bread Board orPCB. 10. Hardware implementation of 6/12 V DC Motor Speed Control(Bidirectional) 11. Simulate Buck, Boost, Buck-Boost circuit and validate on Bread Boardor PCB. 12. Simulate Battery Voltage Level Indicator Circuit and validate on Bread Board or PCB.
4.	ELECTRICAL MACHINE-II LAB	1. To study various types of starters used for 3 phase induction motor. 2. To connect two 3-phase induction motor in cascade and study theirspeed control. 3. To perform load test on 3-phase induction motor and calculate torque,output power, input power, efficiency, input power factor and slip forvarious load settings. 4. To perform no load and blocked rotor test on a 3-phase induction motorand determine the parameters of its equivalent circuits. 5. Draw the circle diagram and compute the following (i) Max. Torque (ii)Current (iii) slips (iv) p. f.(v) Efficiency. 6. Speed control of 3- Φ Induction Motor 7. To plot the O.C.C. & S.C.C. of an alternator. 8. To determine Zs ,Xd and Xq by slip test, Zero power factor (ZPF)/ Potierreactance method. 9. To determine the voltage regulation of a 3-phase alternator by directloading. 10. To determine the voltage regulation of a 3-phase alternator by synchronous impedance method.

		11. To study effect of variation of field current upon the stator current andpower factor of synchronous motor andPlot V-Curve and inverted V-Curveof synchronous motor for different values of loads. 12. To synchronize an alternator across the infinite bus and control loadsharing.
5.	POWER ELECTRONICS LAB	1. Study the comparison of following power electronics devices regardingratings, performance characteristics andapplications: Power Diode,Power Transistor, Thyristor, Diac, Triac, GTO, MOSFET, MCT and SIT. 2. Determine V-I characteristics of SCR and measure forward breakdownvoltage, latching and holding currents. 3. Find V-I characteristics of TRIAC and DIAC. 4. Find output characteristics of MOSFET and IGBT. 5. Find transfer characteristics of MOSFET and IGBT. 6. Find UJT static emitter characteristics and study the variation in peakpoint and valley point. 7. Study and test firing circuits for SCR-R, RC and UJT firing circuits. 8. Study and test 3-phase diode bridge rectifier with R and RL loads. Study the effect of filters. 9. Study and obtain waveforms of single-phase half wave controlled rectifierwith and without filters. Study the variationof output voltage withrespect to firing angle. 10. Study and obtain waveforms of single-phase half controlled bridgerectifier with R and RL loads. Study and show the effect of freewheelingdiode. 11. Study and obtain waveforms of single-phase full controlled bridgeconverter with R and RL loads. Study and show rectification andinversion operations with and without freewheeling diode. 12. Control the speed of a dc motor using single-phase half controlled bridgerectifier and full controlled bridge rectifier.Plot armature voltage versusspeed characteristics 13.13.

6.	DIGITAL ELECTRONICS LAB	1. To verify the truth tables of basic logic gates: AND, OR, NOR, NAND,NOR. Also to verify the truth table of Ex-OR,Ex-NOR (For 2, 3, & 4inputs using gates with 2, 3, & 4 inputs). 2. To verify the truth table of OR, AND, NOR, Ex-OR, Ex-NOR realized usingNAND & NOR gates. 3. To realize an SOP and POS expression. 4. To realize Half adder/ Subtractor & Full Adder/ Subtractor using NAND& NOR gates and to verify their truth tables. 5. To realize a 4-bit ripple adder/ Subtractor using basic half adder/Subtractor & basic Full Adder/ Subtractor. 6. To verify the truth table of 4-to-1 multiplexer and 1-to-4 demultiplexer.Realize the multiplexer using basic gates only.Also to construct and 8-to-1 multiplexer and 1-to-8 demultiplexer using blocks of 4-to-1multiplexer and 1-to-4 demultiplexer. 7. Design & Realize a combinational circuit that will accept a 2421 BCDcode and drive a TIL -312 seven segmentdisplay. 8. Using basic logic gates, realize the R-S, J-K and D-flip flops with andwithout clock signal and verify their truth table. 9. Construct a divide by 2,4& 8 asynchronous counter. Construct a 4-bitbinary counter and ring counter for a particular output pattern using Dflip flop. 10. Perform input/output operations on parallel in/Parallel out and Serialin/Serial out registers using clock. Also exercise loading only one ofmultiple values into the register using multiplexer.
7.	MEASUREMENT LAB	1. Study working and applications of (i) C.R.O. (ii) Digital Storage C.R.O. &(ii) C.R.O. Probes. 2. Study working and applications of Meggar, Tong-tester, P.F. Meter andPhase Shifter. 3. Measure power and power factor in 3-phase load by (i) Two-wattmetermethod and (ii) One-wattmeter method. 4. Calibrate an ammeter using DC slide wire potentiometer.

		5. Calibrate a voltmeter using Crompton potentiometer. 6. Measure low resistance by Crompton potentiometer. 7. Measure Low resistance by Kelvin's double bridge. 8. Measure earth resistance using fall of potential method. 9. Calibrate a single-phase energy meter by phantom loading at differentpower factors. 10. Measure self-inductance using Anderson's bridge.
8.	POWER SYSTEM-I LAB	1. Generating station design: Design considerations, basic schemes and single line diagram of hydro, thermal, nuclear and gas power plants. Electrical equipment for powerstations. 2. Distribution system Design: Design of feeders & distributors. Calculation of voltagedrops in distributors. Calculationof conductor size using Kelvin's law. 3. Study of short term, medium term and long term load forecasting. 4. Sending end and receiving end power circle diagrams. 5. Substations: Types of substations, various bus–bar arrangements. Electrical equipmentfor substations. 6. Study high voltage testing of electrical equipment: line insulator, cable, bushing, powercapacitor, and powertransformer. 7. Design an EHV transmission line 8. Study filtration and Treatment of transformer oil. 9. Determine dielectric strength of transformer oil. 10. Determine capacitance and dielectric loss of an insulating material using Scheringbridge. 11. Flash over voltage testing of insulators.
9.	CONTROL SYSTEM LAB	1. (a) Plot step response of a given TF and system in state-space. Take different values ofdamping ratio and wn naturalundamped frequency.(b) Plot ramp response. 2. To design 1st order R-C circuits and observe its response with the following inputs and 3. trace the curve.(a) Step(b) Ramp (c) Impulse 4. To design 2nd order electrical network and study its transient response for step inputand following

		cases.(a) Under damped system(b) Over damped System(c) Critically damped system. 5. To Study the frequency response of following compensating Networks, plot the graphand final out corner frequencies.(a) Leg Network(b) Lead Network. (c) Leg-lead Network. 6. Draw the bode plot in real time for a Non-Inverting amplifier. 7. Draw the bode plot in real time for an Inverting amplifier. 8. Draw the bode plot for second order transfer function. 9. Draw the bode plot for first order transfer function. 10. Design and analyse Tow- Thomas biquad filter. 11. Design PID controller and also calculate Kp, Ki, Kd for it.
10.	MICROPROCESSOR LAB	1. Study the hardware, functions, memory structure and operation of 8085-Microprocessor kit. 2. Program to perform integer division: (1) 8-bit by 8-bit (2) 16-bit by 8-bit. 3. Transfer of a block of data in memory to another place in memory 4. Transfer of black to another location in reverse order. 5. Searching a number in an array. 6. Sorting of array in: (1) Ascending order (2) Descending order. 7. Finding party of a 32-bit number. 8. Program to perform following conversion (1) BCD to ASCII (2) BCD to hexadecimal. 9. Program to multiply two 8–bit numbers 10. Program to generate and sum 15 Fibonacci numbers. 11. Program for rolling display of message –India‖, –HELLO‖. 12. To insert a number at correct place in a sorted array. 13. Reversing bits of an 8-bit number. 14. Fabrication of 8-bit LED interfaces for 8085 kit through 8155 and 8255. 15. Data transfer on output port 8155 & 8255 & implementation of disco light, running light, and sequential lights on theabove mentioned hardware. 16. Parallel data transfer between two DYNA-85 kit using

		8253 ports. 17. Generation of different waveform on 8253/8254 programmable timer.
11.	SYSTEM PROGRAMMING LAB	1. Basics of MATLAB matrices and vectors, matrix and array operations, Saving and loadingdata, plotting simplegraphs, scripts and functions, Script files, Function files,Global Variables, Loops, Branches, Control flow, Advanced data objects, Multidimensionalmatrices, Structures, Applications in linear algebra curve fitting and interpolation.Numerical integration, Ordinary differential equation. (All contents is to becovered with tutorial sheets) 2. Write a MATLAB program for designing Rheostat. 3. Idea about simulink, problems based on simulink. (All contents is to be covered withtutorial sheets) 4. Write a program to generate Machine Op- code table using two pass Assembler. 5. Single Phase Full Wave Diode Bridge Rectifier With LC Filter 6. Simulate Three phase Half wave diode rectifier with RL load. 7. Starting of A 5 HP 240V DC Motor With A Three-Step Resistance Starter. 8. Simulate OC/SC test of 1-phase transformer. 9. Simulate Torque- speed characteristics of induction motor.
12.	POWER SYSTEM-II LAB	1. Fault analysis (for 3 to 6 bus) and verify the results using MATLAB or any availablesoftware for the cases: (i) LG Fault (ii) LLG Fault (iii) LL Fault and (iv) 3-Phase Fault. 2. Load flow analysis for a given system (for 3 to 6 bus) using (i) Gauss Seidal (ii) NewtonRaphson (iii) Fast DecoupledMethod and verify results using MATLAB or anyavailable software. 3. Three phase short circuit analysis in a synchronous machine(symmetrical faultanalysis) 4. Study of voltage security analysis. 5. Study of overload security analysis and obtain results

		for the given problem usingMATLAB or any software. 6. Study of economic load dispatch problem with different methods. 7. Study of transient stability analysis using MATLAB/ETAP Software. 8. 8. Power flow analysis of a slack bus connected to different loads.
13.	ELECTRIC DRIVE LAB	1. Study and test the firing circuit of three phase half controlled bridge converter. 2. Power quality analysis of 3 phase half controlled bridge converter with R and RLloads. 3. Power Quality analysis of 3-phase full controlled bridge converter feeding R andRL load. 4. Study and obtain waveforms of 3-phase full controlled bridge converter with R andRL loads. 5. Experimental analysis of 3-phase AC voltage regulator with delta connected, starconnected (with floating load), R& RL load 6. Control speed of dc motor using 3-phase half controlled bridge converter. Plotarmature voltage versus speed characteristic. 7. Control speed of dc motor using 3-phase full controlled bridge converter. Plotarmature voltage versus speed characteristic. 8. Control speed of a 3-phase induction motor in variable stator voltage mode using3-phase AC voltage regulator. 9. Control speed of a 3-phase BLDC motor. 10. Control speed of a 3-phase PMSM motor using frequency and voltage control 11. Control speed of universal motor using AC voltage regulator. 12. Study 3-phase dual converter. 13. Study speed control of dc motor using 3-phase dual converter. 14. Study three-phase cyclo-converter and speed control of synchronous motor usingcyclo-converter. 15. 15. Control of 3-Phase Induction Motor in variable frequency V/f constant mode using3-phase inverter.

14.	POWER SYSTEM PROTECTION LAB	1. To determine fault type, fault impedance and fault location during single line toground fault. 2. To determine fault type, fault impedance and fault location during single line-tolinefault. 3. To determine fault type, fault impedance and fault location during double line toground fault. 4. To study the operation of micro-controller based over current relay in DMT typeand IDMT type. 5. To analyse the operation of micro-controller based directional over current relay inDMT type and IDMT type. 6. To study the micro-controller based under voltage relay. 7. To study the micro-controller based over voltage relay. 8. To study the operation of micro-controller based un-biased single-phasedifferential relay. 9. To study the operation of micro-controller based biased single-phase differentialrelay. 10. To study the operation of micro-controller un-based biased three phase differentialrelay. 11. To study the operation of micro-controller based biased three phase differentialrelay.
15.	MODELLING AND SIMULATION LAB	1. Simulate Swing Equation in Simulink (MATLAB) 2. Modeling of Synchronous Machine. 3. Modeling of Induction Machine. 4. Modeling of DC Machine. 5. Simulate simple circuits. 6. (a) Modeling of Synchronous Machine with PSS (b) Simulation of SynchronousMachine with FACTS device. 7. (a) Modeling of Synchronous Machine with FACTS device (b) Simulation ofSynchronous Machine with FACTS devices. 8. FACTS Controller designs with FACT devices for SMIB system.
16.	POWER SYSTEM PLANNING LAB	1. Status of National and Regional Planning, for power system

		2. Write components of Structure of power system 3. Explain in detail various planning tools. 4. Write short note on Electricity Regulation 5. Modeling of Electrical Forecasting techniques 6. Transmission and distribution planning 7. concept of Rational tariffs 8. Rural Electrification
17.	POWER SYSTEM MODELLING AND SIMULATION LAB	1. Simulate Swing Equation in Simulink (MATLAB) 2. Modeling of Synchronous Machine. 3. Modeling of Induction Machine. 4. Simulate simple circuits using Circuit Maker. 5. (a) Modeling of Synchronous Machine with PSS (b) Simulation of Synchronous Machinewith FACTS device. 6. (a) Modeling of Synchronous Machine with FACTS device (b) Simulation of SynchronousMachine with FACTS devices. 7. FACTS Controller designs with FACT devices for SMIB system.
18.	COMPUTER BASED POWER SYSTEM LAB	1. Fault analysis (for 3 to 6 bus) and verify the results using MATLAB or any available software forthe cases: (i) LG Fault (ii) LLG Fault (iii) LL Fault and (iv) 3-Phase Fault 2. Load flow analysis for a given system (for 3 to 6 bus) using (i) Gauss Seidal (ii) Newton Raphson(iii) Fast Decoupled Method and verify results using MATLAB or any available software 3. Study of voltage security analysis 4. Study of overload security analysis and obtain results for the given problem using MATLAB orany software. 5. Study of economic load dispatch problem with different methods. 6. Study of transient stability analysis using MATLAB/ETAP Software.
19.	ELECTRICAL DRIVES AND CONTROL LAB	1. Study and test the firing circuit of three phase half controlled bridge converter. 2. Study and obtain waveforms of 3 phase half

		controlled bridge converter with R and RL loads. 3. Study and test the firing circuit of 3-phase full controlled bridge converter. 4. Study and obtain waveforms of 3-phase full controlled bridge converter with R and RL loads. 5. Study and test 3-phase AC voltage regulator. 6. Control speed of dc motor using 3-phase half controlled bridge converter. Plot armature voltageversus speed characteristic. 7. Control speed of dc motor using 3-phase full controlled bridge converter. Plot armature voltageversus speed characteristic. 8. Control speed of a 3-phase induction motor in variable stator voltage mode using 3-phase ACvoltage regulator. 9. Control speed of a 3-phase BLDC motor. 10. Control speed of a 3-phase PMSM motor using frequency and voltage control 11. Control speed of universal motor using AC voltage regulator. 12. Study 3-phase dual converter. 13. Study speed control of dc motor using 3-phase dual converter. 14. Study three-phase cycloconverter and speed control of synchronous motor using cycloconverter. 15. Control of 3-Phase Induction Motor in variable frequency V/f constant mode using 3-phaseInverter
20.	HIGH VOLTAGE ENGINEERING LAB	1. Study filtration and Treatment of transformer oil. 2. Determine dielectric strength of transformer oil. 3. Determine capacitance and dielectric loss of an insulating material using Schering bridge. 4. Study solid dielectrics used in power apparatus. 5. Study applications of insulating materials. 6. Study direct testing and indirect testing of circuit breakers. 7. Study high voltage testing of electrical equipment: line insulator, cable, bushing, power capacitor,and power transformer. 8. Design an EHV transmission line.

Department of Mechanical Engineering

S. No.	Name of the Laboratory	Experimental Setup Available
1	**CAM Lab**	CNC Lathe Machine
		CNC Milling Machine
2	**I.C.Engine Lab**	Single Cylinder Diesel Engine Test Rig With Rope Brake Dynamometer
		Multi Cylinder Petrol Engine Test Rig (Morse Test) With Hydraulic Dynamometer
		Four Gas Analyzer
		Single Cylinder Diesel Engine Test Rig With Hydraulic Dynamometer
3	**Turbo Machinery Lab**	Vapour Compression Refrigeration System Test Rig
		Pelton Wheel Turbine Test Rig
		Francis Turbine Test Rig
		Centrifugal Pump Test Rig
		Wind Tunnel Test Rig
		Axial Fan Test Rig
4	**Fluid Mechanics Lab**	Meta-Centric Height Apparatus
		Venturi Meter Test Rig
		Orifice meter Test Rig
		Losses Due To Friction In Pipe Lines
		Discharge Over Notches
		Flow Through Orifice And Mouth Piece
		Bernoulli's Theorem Apparatus
		Double Stage Air Compressor Test Rig
5	**Vibration Engineering Lab**	Universal Vibration Testing Machine
6	**Heat Transfer Lab**	Pin Fin Testing Machine
		Thermal Insulator Slab And Insulating Powder Testing Machine

		Heat Transfer Co-Efficient Measuring Device For Conduction
		Emissivity Measuring Device
		Boiling Heat Transfer Device
		Heat Transfer Co-Efficient Measuring Device For Natural Convection
		Heat Pipe Demonstrator
7	**Dynamics Of Machine Lab**	Static & Dynamics Balancing Setup
		Motorized Gyroscope Set up
		Journal Bearing Apparatus
		Wheel Balancing M/c
		Governor Apparatus
8	**Material Science and Testing Lab**	Universal Testing Machine
		Torsion Testing Machine
		Impact Testing Machine
		Fatigue Testing Machine
		Hardness Testing Machine
		Spring Testing Machine
9	**Production Lab**	Lathe Dynamometers
		Lathe Machines
		Milling Machines
		Shaper Machines
		Milling Dynamometer
		Capstan Lathe
		Spot Welding Machine
		Drilling Machines
		Universal Strengthen Machine Hydraulic Vun
11	**BME Lab**	Model of Two-stroke & Four-stroke Diesel Engines.
		Refrigeration Trainer
13	**KOM Lab**	Four Bar Chain
		Double Slider Chain Oldham Coupling
		Cam-Follower Arrangements

		Rope & Brake dynamometers
14	**Thermal Lab**	Four Stroke Petrol Engine And Four Stroke Diesel
		Two Stroke Petrol Engine And Two Stroke Diesel
		Single Cylinder Diesel Engine
		Ignition Systems of an IC Engine
		Lubrication System Of An IC Engine
		Cooling Systems Of An IC Engine

First Year

Sr.No.	**Name of the Laboratory/Workshop**	**Experimental set up available**
1	ENGINEERING PHYSICS LAB	Sextant.
		Energy band gap Determination Kit
		Hall Exp. Setup
		Charging and discharging of a condenser Kit
		Newton's Ring Exp. Setup
		He –Ne laser
		Spectrometer.
2	MECHANICAL WORKSHOP PRACTICE LAB.	Fitting shop
		Carpentry shop
		Machine shop
		Welding shop
		Foundry shop
3.	CIVIL LAB	Dumpy level
		Auto level
		Prismatic compass

		Surveyor compass
		Metric chain
		Steel tape
		Metal tape
		Levelling staff
		Ranging rods
		Tripod for compass
		Tripod for dumpy/auto level
		Laser distance mete
		Fiber glass tape
4	LANGUAGE LAB	Systems: 60 (Pentium 4 – 2.6 Ghz 80 GB Hard Disc)
		Head Phones: 60
		16 Inch TFT
		SoSoftware Used - iTell – Orell Digital Language Lab upgraded to P1 Version for 200 users
5	COMPUTER PROGRAMMING LAB	i3- Desktop- PC
		60-PC Available
6	ENGINEERING CHEMISTRY LAB	Volumetric titration setup
		Redwood Viscometer
		Cloud And Pour Point Apparatus
		Pensky Martins Apparatus
		Digital conductivity meter
		Electric oven
		Muffle furnace

Annexure-7

Special purpose facilities available

Department of Electronics & Communication Engg

1) Robotics Research and Development cell

It provides the platform to design and develop various robots such as Humanoid robot and 18 DOF hexapod with help of 3 D printers and 3D scanners available with different bed sizes.

2) Electronic Skill Development Center

Electronics Skill Development Centre helps in imparting of outcome oriented skills and development of various kits for the Electronics Systems, Design and Manufacturing (ESDM) Industry. like Half wave rectifier, Full wave center taped rectifier etc

3) Center Of Excellence in Optical Fiber Communication

a) It provides platform to design and identify components of Optical Fiber cable, splice closures, Single mode and multimode pig tails and patch cord, tool kit for splicing etc

b) Identification and use of different tools for end preparation of Optical Fiber cable.

4) State of the Art LED lab

ECE Research and Design Center- The State of the Art LED Cell help students to implement innovative projectideas based on LED.

• To enhance further developments in energy efficiency, luminance and the availability of wave lengths

7) IoT Lab

The Internet of Things (IoT) Lab helps students with the concept that describes the idea of everyday physical objects being connected to internet and being able to identify themselves to other devices.

Department of Computer Science and Engineering

Special Lab

- **Android Application Development Lab**
- **Cloud Computing Lab supported by Redhat Academy**
- **Oracle WDP Lab: Database Lab and Java Programming Lab**
- **Data Analytics Lab**
- **Spoken Tutorial Lab**

Specific Facilities Provided in Project Laboratory

S.No.	Facility
1.	Special lab with systems is provided for carrying out project work.
2.	Every project group has been allotted with guide in order to pursue with theirproject work.
3.	Licensed software"s and software"s downloaded from open source are provided to Students according to their requirements.
4.	Training programs are conducted to initiate their project work.
5.	Network and internet facilities are provided to students.
6.	Digital library facility with access to Journals has been extended to thestudents.
7.	Instructors will assist students to setup their systems/ laptops to start their projectwork.
Sponsored Projects	
1.	Guidance given to students to apply for the Government sponsored projects like DST.
2.	Memorandum of Understanding (MOU) between various industry and professional societies is Established. And students are promoted and guided to work on live projects tosolve problems of common man.
3.	Live projects sanctioned for the benefit of students.
4.	Software Development Club/ EDC Cell is formed to encourage students to apply for live projects.

5.	Awareness program / Seminar to specify about procedure, guidelines to apply for DST are conducted by project coordinator.
6.	Project guides and project coordinators constantly encourage students to participate in project exhibitions and coding competitions like HACKATHON,RTU-THAR,TOP CODER,Hackerearth, Hacker Rank, etc.

Project Lab:

- **Android Application Development Lab**

This Project Lab is for Development of Mobile Technology Platforms & to provide Solutions for Problems from Social, Governance, Education and Rural development Domain.

In the context of Social, Governance, Education and Rural development Domainit is required to pursue and achieve goals directly related to the creation of value for the Citizens, Students, Rural development, and societal information support system. The focus is on improving the "flow" or smoothness of information acquisition and dissemination.

The implementation of smoothness of information acquisition and dissemination in above mention domain, reduces service and information propagation time results as a consequence. The system uses Android SDK, android studio and peer user model.

Objectives:

- Develop Technology platforms for Effective information dissemination
- Solutions to present Visualization of information flow, capacity utilization, manpower development , social up-liftmen, effective learning, good governance
- To develop rapid prototyping approaches for replication of the solution across Social, Governance, Education and Rural development Domain
- To create and design implementation solution, technology platform for Problems from various Hackathon, Business requirements

Industry oriented Labs:

As be focus on imparting industry oriented education to our students so that they will be ready to face the challenges of industry culture after completing their graduation. We prepare them as ready to use products rather than a product in testing phase. For achieving this we have also established few research oriented labs based on latest technologies in demand in industry in association with our industry MOU"s.

- **Cloud Computing Lab supported by Redhat Academy**

Laboratories are important to engineering and technology curricula. Through systematically designed experiments, research scholars and students can gain hands-on experience, enhance classroom learning, and cultivate career interests. Thus, how to effectively extend laboratories via cyberspace and maximize resources utilization has caused many researchers‟ attention. In recent years, Cloud Computing technology has developed drastically, which provided an ideal solution for virtual and remote laboratory implementation. Our focus in cloud computing research lab is to provide facility for further enhancement in technology and experience in experimentation. It is a combined research lab for UG and PG students of CSE and Information Technology.

Focus Areas:

- Virtual Machine Management.
- Storage Management.
- Data routing and Datacenter Networking.
- Simulation of MANET and data mining

- **Oracle WDP Lab: Database Lab and Java Programming Lab**

Oracle is computer application software that provides a way to manage data. The requirement of modern days is to have an automated system that manages, modifies and updates data accurately. This is achieved by a DBMS in robust, correct and non-redundant way. Oracle lab aims at practicing and achieving this aim by using various software‟s such as SQL, ORACLE, and MS – Access etc. All these require a thorough practice of various DDl, DCL and DML queries.

The Java Programming Language is a general-purpose, concurrent, strongly typed, class-based object-oriented language. The aim of this lab is to help students learn Java Programming step by step. It is compiled to the bytecode (platform independent code) instruction set and binary format defined in the Java Virtual Machine Specification. The latest Java Development Kit (JDK) has been installed with all the new features that support advanced programming. JAVA has always been the best choice for most of the mobile applications.

Objectives:

- To build software development skills using java programming for real world applications.
- To implement frontend and backend of an application.
- To implement classical problems using java programming.

- **Data Analytics Lab:**

Python is a general-purpose programming language that is becoming more and more popular for doing data science. Companies worldwide are using Python to harvest insights from their data and get a competitive edge. Unlike any other Python tutorial, this course focuses on Python specifically for data science. In data analytics lab, students will learn about powerful ways to store and manipulate data as well as to use data science tools to start data analysis.

Objective:

- To use Python both interactively and through a script.
- Learn to store, access and manipulate data in lists.
- Learn to work with the Anaconda, a powerful tool in data exploration.

Department of Electrical Engineering

Industrial Support Labs

PLC/SCADA Lab- Connecting the dots between Education and Industry, this lab offers the best to learn in Industrial Automation Technology. Either it is *Siemens* ET200S PLC controlling 13 different projects like Mixing Plant, Coal Crusher, Smart City or Automated Water Treatment and Distribution System, Wireless Pick Drop Robot etc. prepares the Student to be „Future Ready".

High Voltage Engineering Lab- A unique *State-of-the-Art* 100KV High Voltage Testing Set-Up facilitates the testing of Cables, Insulators and Corona. Also being equipped with Transformer Oil Filtration and Oil Testing, Buchholz Relay, Transmission Line Simulation System etc gives an edge to the Skills of Student.

Grid Sub-Station- The Ultimate 4 Point *PLC* Controlled 1.1KV Hybrid Grid Sub-Station gives the glimpse of remarkable efforts should be put in to achieve the best. Another barrier breaking learning to make student‟s knowledge shine more.

INCUBATION CENTRES

Skill Development Cell- Applying the knowledge to satisfy the need of Consumer is the intention used to design this Lab. Making student learn, apply and deliver even up to the basic level by designing and fabrication of lighting products like CFL and LED, Circuits of RO and Inverter with the help of well equipped Work-Station and 45 point Test Rig motivates Students to stand on Own.

Solar Lab- Adapting the Change in Technology while respecting the Nature is in it‟s Core. Student goes through the process of understanding different types of Solar Plates and Solar Cells. The 60W Series and 70W Parallel demonstration set ups, Solar Wheel Chair, Solar Bicycle, etc encourages student to explore the latest in technology.

Research & Development

MATLab- An idea should be put to test to qualify for real. Student design and test circuits on software to look for desired Output. Analysis can be done on simulation where results could be graphical, statistical etc for improvisation to find more efficient and convenient ways to deliver the best.

❖ **Digital Library/ The E-Journals/E-Resources details are as under:**

Sr. No.	E-Journal	Access Link
1	DELNET	Go to- http://delnet.nic.in

ANDRIOD APPLICATION DEVELOPMENT LAB

Development of Mobile Technology Platforms &Solutions for Problems from Social, Governance, Education and Rural development Domain

In the context of Social, Governance, Education and Rural development Domainit is required to pursue and achieve goals directly related to the creation of value for the Citizens, Students, Rural development, and societal information support system. The focus is on improving the "flow" or smoothness of information acquisition and dissemination.

The implementation of smoothness of information acquisition and dissemination in above mention domain, reduces service and information propagation time results as a consequence. The system uses Android SDK, android studio and peer user model.

OBJECTIVES

Develop Technology platforms for Effective information dissemination

- Solutions to present Visualization of information flow, capacity utilization, manpower development, social up-liftment, effective learning, good governance
- To develop rapid prototyping approaches for replication of the solution across Social, Governance, Education and Rural development Domain
- To create and design implementation solution, technology platform for Problems from various Hackathon, Business requirements

Implementation:

Students of final year have to identify projects from above domain from Smart India Hackathon (SIH) or any other top rated Hackathon or from industry sponsored problem. They are allowed to work in team of 8 as per SIH guidelines. They are allotted a workplace and workstation to work on problem and it‟s solution after approval of suggested solution as per SIH guideline. Selected team for SIH or any other top rated Hackathon finale are assigned alumni as mentor who are from industry and rest are assigned to faculty mentor.

S.No.	Facility
1	Special lab with systems is provided for carrying out project work.
2	Every project group has been allotted a guide in order to pursue various task within the project work.
3	Licensed software‟s and software‟s downloaded from open source are provided tostudents according to their requirements.
4	Training programs are conducted to initiate their project work.
5	Network and internet facilities are provided to students.
6	Digital library facility with access to Journals has been extended to thestudents.
7	Instructors will assist students to setup their systems/ laptops to start their project work.
Sponsored Projects	
1	Guidance given to students to apply for the Government sponsored projects like DST.
2	Memorandum of Understanding (MOU) between various industry and professional societies is Established. And students are promoted and guided to work on live projects tosolve problems of common man.
3	Live projects sanctioned for the benefit of students.
4	Software Development Club/ EDC Cell is formed to encourage students to apply for live projects.
5	Awareness program / Seminar to specify about procedure, guidelines to apply for DST / IBM Projects, are conducted by project coordinator.
Project Exhibitions	
1.	Project guides and project coordinators constantly encourage students to participatein project exhibitions and coding competitions like HACKATHON,RTU-THAR,TOP CODER,Hackerearth, Hacker Rank, etc.

Facilities Provided in Project Laboratory

Impact:

The Project lab has good impact which is as follows:

1. Major participation and maximum selection (as per cap per institute) in Smart India Hackathon grand finale since inception.
2. A good number in adaption of developed apps.
3. Some apps developed are in early phase of Incubation.
4. Some apps developed are funded by state DST

Annexure-8

INTERNAL CONTINUOUS EVALUATION SYSTEM IN PLACE

Quality of Classroom Teaching

The following innovative teaching methods are adopted by the faculty members in the class:

- The first lecture of the semester commences with an introductory class in which faculty members stresses upon the class room management, class ambiance, general discipline and dress code etiquettes. Faculty introduces themselves and interacts with students. Course Objectives, Course Outcomes, Evaluation Scheme, Syllabus and importance of the concerned subject in Industry and likely career avenues are discussed.
- Every lecture starts with the discussion on the previous day's discussion and doubts are clarified. This makes students more attentive to what a faculty is teaching in the class.
- Faculty members randomly review the notebooks of students. The art of note-taking and summarizing empowers the student to perform better and also enhances the classroom teaching experience.
- Faculty members manage the classroom rather than just teaching a class. They organize classroom, manage the curriculum and keep students on task with various management techniques.
- Students are taught critical thinking skills rather than just teaching them to memorize facts hence students improve in other areas as well.
- Course files are prepared before the commencement of semester in which lecture plan, lecture delivery schedule, assignments plan, various assignments/quizzes/tests with solutions/answer keys, previous year question papers etc. are the main ingredients. The lecture plan, evaluation scheme, Course Outcomes etc are shared with the students by respective faculty members so that students may schedule their activities accordingly.
- The faculties make the students understand the concept/principles/ theory / problems in the classroom, keeping in view various cognitive levels of learning. This enriches the quality of teaching and leads students towards fast learning in the classroom environment.
- Faculty members use active learning in the class so that students can understand, learn and remember the complex concepts of engineering at ease.
- Students are also involved in cooperative learning which involves students working in a team to accomplish assigned task.
- Assessment and evaluation of teaching quality is done by head of the department. HOD takes students feedback at different interval of time and accordingly plans the actions to improve teaching learning process.

Quality of internal semester Question papers, Assignments and Evaluation

Internal Assessment marks set as per RTU regulations is 20 for theory and 60% of total practical marks, 100 for seminar while it is 250 for project. The internal assessment marks for theory is based on two midterm tests conducted as per the calendar of events. Program Coordinator along with test coordinator is responsible for the conduction of the test

Departmental Internal Examination cell is constituted which will look into the authenticity of the question paper. The committee consists of four members:

- Head of the department as Chairperson
- 1 Professor as member
- 2 senior faculties as members

The regulations, curricula and syllabi of all the programmes offered by the Institute are available in the Institute and the affiliated University websites. The regulations contain the details of the evaluation process. The Officer-In-Charge of the Examination Cell of the Institute has prepared an Instruction Manual as per the guidelines of the Controller of Examination of RTU to conduct of examinations and copies are available to all departments.

The Examination Cell of the Department deals with the internal examination process. The following efforts were made in the office of the Examination Cell for smooth conduct of the examination and related processes. Preparing Academic calendar with the schedule of internal assessment test and end semester examinations for both theory and laboratory courses, Preparation of Schedules for two Midterm tests and publication of result. Disbursal of necessary materials to the internal examiners through the Administrative office of the college. Preparing a) The attendance sheet b) Invigilator schedule c) Physical arrangements and related matters

The Schedule of Examinations and Academic calendar and other information related to the conduct of examinations are published on the departmental notice boards.

Initiatives and Implementation details for improving the quality of Internal Semester

I. Quality of Internal Assessment Test (IAT) paper:

1. Every course has a coordinator – course coordinator who is responsible for the setting of the question paper. For designing and evaluating internal assessment test and assignments we adhere to follow Bloom's Taxonomy. Questions are designed as per Bloom's knowledge level following the university pattern.
2. Course coordinator ensures that the question paper should be as per bloom taxonomy.
3. The syllabus pertaining to the respective IAT is announced well before the commencement of the same.

4. The question paper is set for 20 marks and the duration is 1 hour 30 Minutes.
5. Two sets of internal semester examination's question papers are set up by the respective subject teachers considering University pattern and last 5 years University question papers. Importance of the topics with respect to the learning/ course outcome is taken into consideration. The mapping of every question with course outcome is also prepared to check for the equal coverage of all Co's.
6. The question paper is submitted to the program coordinator through test coordinator along with scheme and solution one week prior to the commencement of the test.
7. This is forwarded to the Examination cell by the Program coordinator
8. The Examination cell constituted will look into the paper and give their opinion about the same. If the question paper needs to be relooked into for any reason – the same is bought to the notice of the course coordinator; other-wise paper accepted is handed back to the program coordinator.

❖ **Assessment Pattern**

Assessment tools	**Marks**
Test 1	Average of two 20
Test 2	
Final Exam	80
Total	**100**

- **Evaluation**
- After examination, solution of the question paper with proper markings is shared with the students. The solution is disseminated among students through direct discussion in the class.
- After evaluation of answer sheets, all faculty members prepare the gap analysis in terms of the performance of students in their courses and corrective action is taken for every gap found.
- Evaluated answer sheets are shown to students and discussion is done in the class.

❖ **<u>Distribution of knowledge levels of Bloom's taxonomy</u>**

For Written Examinations (only mid terms), Practical Examinations (only internal test) we follow **Bloom's taxonomy** for designing balanced question paper consisting of questions of different knowledge levels as follows:

Level K-1: Knowledge

Knowledge involves recognizing or remembering facts, terms, basic concepts, or answers without necessarily understanding what they mean. Its characteristics may include:

- Knowledge of specifics—terminology, specific facts

- Knowledge of ways and means of dealing with specifics—conventions, trends and sequences, classifications and categories, criteria, methodology
- Knowledge of the universals and abstractions in a field—principles and generalizations, theories and structures

Level K-2: Comprehension

Comprehension involves demonstrating and understanding of facts and ideas by organizing,comparing, translating, interpreting, giving descriptions, and stating the main ideas.

Level K-3: Application

Application involves using acquired knowledge—solving problems in new situations by applying acquired knowledge, facts, techniques and rules. Learners should be able to use prior knowledge to solve problems, identify connections and relationships and how they apply in new situations.

Level K-4: Analysis

Analysis involves examining and breaking information into component parts, determining how the parts relate to one another, identifying motives or causes, making inferences, and finding evidence to support generalizations. Its characteristics include:

- Analysis of elements
- Analysis of relationships
- Analysis of organization

Example: List four ways of serving foods made with apples and explain which ones have the highest health benefits. Provide references to support your statements.

Level K-5: Synthesis

Synthesis involves building a structure or pattern from diverse elements; it also refers to the act of putting parts together to form a whole. Its characteristics include:

- Production of a unique communication
- Production of a plan, or proposed set of operations
- Derivation of a set of abstract relations

Level K-6: Evaluation

Evaluation involves presenting and defending opinions by making judgments about information, the validity of ideas, or quality of work based on a set of criteria

- Internal Tests are conducted and records are shown. Any doubt about test copy evaluation is made clear to the students.

- Whenever class tests and Unit tests are taken the results of the student's performance are shown to the students to encourage them or counsel them for better future performance.
- Regular assignments are given and answers are discussed in the class.

II. <u>Quality of Assignment and its relevance to COs:</u>

- For improving the performance of students especially weak students subject assignments are given by the faculty.
- Assignments improve self-learning and help in practicing the exam pattern.

- Every faculty member is expected to give assignments at regular intervals of their course coverage.
- At least, two assignments for every subject are prepared by respective course faculty member. The assignment consists of thought provoking questions and contains theory as well as practical content.
- Assignment issue and submission dates are announced by the respective faculty members.
- Assignment questions are prepared in accordance with RTU pattern of questions following Knowledge levels of Bloom's Taxonomy.
- The assignment along with its solution/answer key is kept in course file. Students submit the solution of the assignment within a week. After that, solution is discussed with the students.
- Assignments are evaluated by faculty members, remarks are given and returned back to the students. Assignments are kept by the students themselves.

III. Laboratory Experiments (Assignments)

- The students are motivated to participate in Programming contests as Hackerearth, Hacker Rank, Top Coder, Code vita, Hackathon, etc.
- The college organize inter collegiate contests to encourage students to demonstrate their programming skills.
- The Computer Science & Engineering Laboratories are conducted in session of 3 hours, in each session the faculty explains the logic and (or) algorithm of the program to be experimented.
- The students will write the complete program in concerned programming language in the observation book, and then code/debug/execute the program on the system and interpret the results.
- The executed program with output, related theory and Algorithm or flowchart is documented in the record book by the students later.
- In each subject many students are made to work on number of additional programs for the better understanding of the subject.

- Online Quizzes were conduction at the ending of laboratory sessions to improve the programming skills of the students.

Evaluation:

- Each course, both theory, practical and project work are evaluated for a maximum of marks as per scheme given by University. The project work is evaluated for a maximum of 250 marks.
- For all theory and practical courses the continuous internal assessment carrying 20% marks for theory mid-term examination and 60% marks of practical examination are subdivided to conduction of laboratory experiment and attendance record (20% marks), performance in laboratory class (20% marks), viva-voice (20% marks) respectively while the end semester examination shall carry 80 marks for theory and 40% marks practical respectively.

Impact analysis

- The academic performance has witnessed an upward swing over the years. Many students did excellence in academics and topped in university.
- Students can focus on segmented marking system to earn better score.
- Class attendance has been improved, because the students become more serious to attend regular classes as the evaluation system contains internal marks for good attendance
- Both theory and practical parts are being emphasized and students doing well in higher studies and employment fields.
- Improvement in analytical abilities of students thus improves the placement

Result

- For the internal tests the results are declared within 7 days after the last examination.
- For end semester examination, the results are declared by the Affliating University normally within 30-60 days after the last examination.

STUDENTS ASSESSMENT OF FACULTY

The feedback collection process is very important for the improvement of the Institution. The faculty feedback is collected from the students every semester. This process contributes to evaluate faculty performance for reward / corrective measures. The feedback forms are given to the students during the regular class hours and collected by the inter department faculty.

Specify the feedback collection process : Manual

Average Percentage of students who participate : More than 75% students

Specify the feedback analysis process :

The inter department faculty collect the feedback forms and prepare the consolidated Report. Which is forwarded to the Principal Office for further Corrective measures and the same is sent to respective HOD's.

- Nominated Faculty members other than the department will conduct the feedback during the semester
- The performance attributes and the subject knowledge and delivery is being concentrated mostly.
- The way in which the subject is introduced and taught to the students could be analyzed, assessed meticulously.
- The feedback is communicated to the faculty along with suggestions / improvements / modifications (if any)

Corrective Actions taken:

- The faculties performing below average are trained continuously through **Faculty Development Programme** to improve their teaching quality.
  The teaching performance indices are analyzed by the Principal office and the same is conveyed to the concerned.

Basis of reward / corrective measures:

There is well defined FPAS system for rewards/corrective measures.

System of Reward:

- Basis of reward/corrective measures, if any : YES
- Any extraneous factors, like hard /soft-attitude of the instructor considered :YES
- Is result considered :YES

Best performing faculty is rewarded by issuing a letter of appreciation. Performance rating of faculty through student feedback system is one of the factors in evaluating the annual performance and to release the annual increments.

Annexure-09

Special Purpose Softwares

Department of Computer Science and Engineering

S.No.	Name of the Facilities	Utilization
1.	Turbo C 3.0,	3rd&6th semester students Software Engineering & Computer Graphics Lab respectively, PG students, Research scholars and Faculty members.
2.	Fedora , Red Hat Linux	4th, 7th,8th semester students, PG students, Research scholars and Faculty members.
3.	Java SE Development Kit Microsoft Visual Studio ,	4th, 7th,8th semester students, PG students, Research scholars and Faculty members.
4.	My Eclipse, Net beans IDE	7th,8th semester students, PG students, Research scholars and Faculty members,.
5.	Apache Tomcat	7th, 8th semester students, PG students, Research scholars and Faculty members.
6.	Microsoft Office professional , Adobe Reader	6th, 7th, 8th semester students, PG students, Research scholars and Faculty members.
7	My Sql,	6th, 7th, 8th semester students, PG students, Research scholars and Faculty members.
8	Python Lab (Anaconda)	6th, 7th, 8th semester students, PG students, Research scholars and Faculty members

Department of Mechanical Engineering

S. No.	Design Softwares	Details
1	Auto Cad	Open software
2	CREO	Open software

All India Council for Technical Education
(A Statutory body under Ministry of
Education, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070Website:www.aicte-india.org

APPROVAL PROCESS 2024-25

Extension of Approval (EoA)

F.No. North-West/1-43664485127/2024/EOA DateofApproval:23-

Mar-2024 To,

The Principal Secretary (Technical)
R.No.1135,MainBuilding,
Secretariat, Jaipur-302005

Sub: Extension of Approval for the Academic Year 2024-25

Ref:OnlineapplicationoftheInstitutionsubmittedforExtensionofApprovalfortheAcademi

cYear2024-25 Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Education), Powers delegatedinAICTEACT1987,(No52of1987)chapterII-u/s2(g)toregulateTechnicalandsubsequentRegulationsofAICTE,Iam directed to convey the approval to:

Permanent Id	1-5979304	**Application Id**	1-43664485127
Name of the Institution	VEDANT COLLEGE OF ENGINEERING&TECHNOLOGY	**Name of the Society/Trust**	SANWARIAPUBLICSCHOOL SAMITI
Institution Address	VILLAGE:TULSI,P.O:-JAKHMUND, DISTT:- BUNDI, BUNDI, BUNDI, Rajasthan, 323021	**Society/Trust Address**	,AJMER,AJMER,Rajasthan,
Institution Type	Private-Self Financing	**Region**	North-West
Year of Establishment	2008		

To conduct following Programs/Courses with the Intake indicated below for the Academic Year 2024-25

Level	Program	Course	AffiliatingBody (University /Body)	Intake Approved for2023-24	Intake Approved for2024-25	NRI Approval Status	FN / Gulf quota/OCI/ Approval Status
DIPLOMA	ENGINEERING AND TECHNOLOGY	CIVIL ENGINEERING	BoardofTechnical Education And Directorate Of Technical Education,Jodhpur	60	60	No	No
DIPLOMA	ENGINEERING AND TECHNOLOGY	ELECTRICAL ENGINEERING	BoardofTechnical Education And Directorate Of Technical Education,Jodhpur	120	120	No	No
DIPLOMA	ENGINEERING AND TECHNOLOGY	MECHANICAL ENGINEERING	BoardofTechnical Education And Directorate Of Technical Education,Jodhpur	30	30**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	CIVIL ENGINEERING	Rajasthan Technical University,Kota	30	30**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER ENGINEERING	Rajasthan Technical University,Kota	30	30	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRICAL AND ELECTRONICS ENGINEERING	Rajasthan Technical University,Kota	60	60	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRICAL ENGINEERING	Rajasthan Technical University,Kota	60	60	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRONICS& COMMUNICATION ENGG	Rajasthan Technical University,Kota	15	15**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	MECHANICAL ENGINEERING	Rajasthan Technical University,Kota	30	30	No	No
POST GRADUATE	ENGINEERING AND TECHNOLOGY	POWER SYSTEMS	Rajasthan Technical University,Kota	18	18	No	No
POST GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER SCIENCEAND ENGINEERING	Rajasthan Technical University,Kota	9	9	No	No

**Intake reduced due to the admissions less than or equal to 30% of the initial "Approved Intake" for the past 5 years consistently

AllAICTEapprovedInstitutionsareempoweredtonurtureecosystemsforSkilling(throughVocationalcourses)viamakingeffectiveuseof existing infrastructure facilities and human resources.

It is mandatoryto comply with all the essentialrequirementsasgiven in APH2024-25to 2027(Chapter-VI)

Important Instructions

1. AspermandatoryDisclosureofAPH2024-27(Annexure-18,page180)Institutionsmustdisclosethefollowinginformation submitted to Council at the Prominent location on its website.
   i. Departmentwiseavailabilityof Infrastructure alongwithapprovedcoursesandintakeapprovedby the Council.
   ii. Facultydetails:Departmentwise:Name&Designationofthefacultymembers/teachingstaffalongwiththeirqualification, tenure of service in your organization, total experience, Institution should also disclose Student Faculty Ratio, Cadre Ratio.
   iii. AdditionallyAuditedFinancialStatements for last 3 Financialyears.
2. Reservation Policy of the Central Government (Including EWS) / Respective State Government/ UT as the case shall be applicableto all the Programmes. The concerned State Government/ UT Admission authority shall decide Modalities of Admission.
3. TheInstitutionofferingcoursesearlierintheRegularShift,FirstShift,SecondShift/PartTimearenowamalgamatedastotal intake and shall have to fulfil all facilities such as Infrastructure, Faculty and other requirements as per the norms specified in the ApprovalProcessHandbook2024-25to 2027for the Total ApprovedIntake.
4. In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approvedby the **Executive Council / General Council as available on the record of AICTE shall be final and binding.**
5. AllAICTEinstitutionsarehighlyencouragedtogetNBA/NAACaccreditation.AlleligibleAICTEinstitutionsarethoroughly encouraged to participate in NIRF ranking process.
6. Deemed to be University: Institutions Deemed to be Universities (Running Technical Education Programmes), it is mandatory to haveAICTEapprovalfromtheAcademicYear2018-19incomplianceoftheHon'bleSupremeCourtOrderdated03-11-2017 passedinCA No.17869-17870/2017.
7. AICTE ApprovedInstitutes areencouragedto utilizeSWAYAM PLUSCoursesup-to40%
8. Internshipis mandatoryfor alladmittedstudents.
9. AICTE ApprovedInstitutes areencouragedto makeefficientuseof the flagshipschemeslike:
   a. Parakh:StudentGap analysisportalbasesservices.
   b. StudentsScholarshipschemeslikePragati,Saksham,Swanath,ADF, etc.
   c. CourseinIndianLanguages.
   d. ATAL FDPs: Faculty trainingfor EmergingareasandcuttingedgeTechnologies.
   e. AugmentingUtilizationof ResearchAssets (AURA).
   f. Smart IndiaHackathon:World'slargestOpenInnovationPlatform.

Prof.RajiveKumar
Member Secretary, AICTE

Copy to:

1. The Director Of Technical Education**, Rajasthan
2. **The Registrar**,**
   Rajasthan Technical University, Kota

3. The Principal / Director,
   VEDANT COLLEGE OF ENGINEERING &TECHNOLOGY
   Village:Tulsi,P.O:-Jakhmund,Distt:-
   Bundi, Bundi,Bundi,
   Rajasthan,323021

4. The Secretary / Chairman,

   AJMER,AJMER
   Rajasthan,

5. Guard File(AICTE)

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

**IndividualApprovallettercopywillnotbecommunicatedthroughPost/Email.However,aconsolidatedlistofApprovedInstitutions(bulk)maybedownloadedfrom the respective login id's.

This is a computer generated Statement. No signature Required

All India Council for Technical Education
(A Statutory body under Ministry of
Education, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2023-24

Extension of Approval (EoA)

F.No. North-West/1-36544920724/2023/EOA Date: 15-May-2023

To,

The Principal Secretary (Technical)
R. No. 1135, Main
Building,
Secretariat, Jaipur-
302005

Sub: Extension of Approval for the Academic Year 2023-24

Ref: Online application of the Institution submitted for Extension of Approval

for the Academic Year 2023-24Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Education) Regulations, 2020notified on 4th February 2020 and amended on 24th February 2021 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to:

Permanent Id	1-5979304	**Application Id**	1-36544920724
Name of the Institution	VEDANT COLLEGE OF ENGINEERING & TECHNOLOGY	**Name of the Society/Trust**	SANWARIA PUBLIC SCHOOL SAMITI
Institution Address	VILLAGE: TULSI, P.O:- JAKHMUND, DISTT:- BUNDI, BUNDI, BUNDI, Rajasthan, 323021	**Society/Trust Address**	,AJMER,AJMER,Rajasthan,
Institution Type	Private-Self Financing	**Region**	North-West
Year of Establishment	2008		

To conduct following Courses with the Intake indicated below for the Academic Year 2023-24

Level	Program	Course	Affiliating Body (University /Body)	Intake Approved for 2022-23	Intake Approved for 2023-24	NRI Approval Status	FN / Gulf quota/ OCI/ Approval Status
DIPLOMA	ENGINEERING AND TECHNOLOGY	CIVIL ENGINEERING	Board of Technical Education And Directorate Of Technical Education, Jodhpur	60	60	No	No
DIPLOMA	ENGINEERING AND TECHNOLOGY	ELECTRICAL ENGINEERING	Board of Technical Education And Directorate Of Technical Education, Jodhpur	120	120	No	No
DIPLOMA	ENGINEERING AND TECHNOLOGY	MECHANICAL ENGINEERING	Board of Technical Education And Directorate Of Technical Education, Jodhpur	60	30**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	CIVIL ENGINEERING	Rajasthan Technical University, Kota	60	30**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER ENGINEERING	Rajasthan Technical University, Kota	30	30	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRICAL AND ELECTRONICS ENGINEERING	Rajasthan Technical University, Kota	60	60	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRICAL ENGINEERING	Rajasthan Technical University, Kota	60	60	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRONICS & COMMUNICATION ENGG	Rajasthan Technical University, Kota	30	15**	No	No
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	MECHANICAL ENGINEERING	Rajasthan Technical University, Kota	30	30	No	No
POST GRADUATE	ENGINEERING AND TECHNOLOGY	POWER SYSTEMS	Rajasthan Technical University, Kota	18	18	No	No
POST GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER SCIENCE AND ENGINEERING	Rajasthan Technical University, Kota	9	9	No	No

**Intake reduced due to the admissions less than or equal to 30% of the initial "Approved Intake" for the past 5 years consistently

It is mandatory to comply with all the essential requirements as given in APH 2023-24 (Appendix 6)

Important Instructions

1. The State Government/ UT/ Directorate of Technical Education/ Directorate of Medical Education shall ensure that 10% of reservation for Economically Weaker Section (EWS) as per the reservation policy for admission, operational from the Academic year 2019-20 is implemented without affecting the reservation percentages of SC/ ST/ OBC(NCL) / General. However, this would not be applicable in the case of Minority Institutions referred to the Clause (1) of Article 30 of Constitution of India. Such Institution shall be permitted to increase in annual permitted strength over a maximum period of two years.

2. The Institution offering courses earlier in the Regular Shift, First Shift, Second Shift/Part Time are now amalgamated as total intakeand shall have to fulfil all facilities such as Infrastructure, Faculty and other requirements as per the norms specified in the Approval Process Handbook 2023-24 for the Total Approved Intake. Further, the Institutions Deemed to be Universities/ Institutions having Accreditation/ Autonomy status shall have to maintain the Faculty: Student ratio as specified in the Approval Process Handbook.

3. Strict compliance of Anti-Ragging Regulation, Establishment of Committee for SC/ ST, Establishment of Internal Committee (IC), Establishment of Online Grievance Redressal Mechanism, Barrier Free Built Environment for disabled and elderly persons, Fire and Safety Certificate should be maintained as per the provisions made in Approval Process Handbook and AICTE Regulation notifiedfrom time to time.

4. In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

5. As per the AICTE Notification dated 29.01.2014 and amended thereto, it shall be mandatory for each Technical Education Institution, University Department and Institution Deemed to be University imparting Technical Education to get accreditation (NBA) for at least 60% of the eligible courses in the next ONE (1) Years' time, otherwise EoA for the subsequent Academic Year (A.Y. 2024-25) shall notbe issued by the Council.

6. Deemed to be University**:** Institutions Deemed to be Universities (Running Technical Education Programmes), it is mandatory to have AICTE approval from the Academic Year 2018-19 in compliance of the Hon'ble Supreme Court Order dated 03-11-2017 passed in CA No.17869- 17870 /2017.

Prof.Rajive Kumar Member Secretary, AICTE

Copy to:

1. The Director Of Technical Education**, Rajasthan
2. **The Registrar**,**
   Rajasthan Technical University, Kota
3. The Principal / Director,
   VEDANT COLLEGE OF ENGINEERING & TECHNOLOGY
   Village: Tulsi, P.O:- Jakhmund, Distt:-
   Bundi,Bundi,Bundi,
   Rajasthan,323021
4. The Secretary / Chairman,

   AJMER,AJMER
   Rajasthan,
5. Guard File(AICTE)

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

VEDANT COLLEGE OF ENGINEERING & TECHNOLOGY, BUNDI

(A Unit of Sanwaria Public School Samiti)

BALANCE SHEET

(As on 31st March, 2024)

Liabilities	Amount (Rs.)	Amount (Rs.)	Assets	Amount (Rs.)	Amount (Rs.)
CAPITAL ACCOUNT		**129536356.64**	**FIXED ASSETS**		**152853034.08**
Corpus Fund	132991656.02		Air Conditioner	35700.00	
Add : Surplus During the year	-3455299.38		Almirah	40100.00	
			Biometric Machine	34000.00	
SECURED LOANS		**19891369.86**	Books	2689259.01	
Bank OD	7,600,404.00		Building	84299734.78	
Secured Loans	12290965.86		Building Under Contruction	9099940.00	
			Car (Toyota)	2833600.00	
UNSECURED LOANS	25669135.87	**25669135.87**	CCTV & DVR	208881.00	
			Ceiling Fan	23000.00	
CURRENT LIABILITIES		**8578334.00**	Computer	14319608.58	
Audit Fee Payable	303517.00		Digital Finger Print Machie	34000.00	
Caution Money	2760500.00		Drill Machine	9362.00	
Hostel Security	189100.00		Epbex & Camera	197549.00	
Salary Payble	754140.00		Exaust Fan	24298.30	
Sundry Creditors	4571077.00		Finger Touch Board	370000.00	
			Fingerprint Scanner	2690.00	
BRANCH/DIVISIONS		**-6439749.69**	Furniture & Fixtures	7645762.02	
Satyam ITI Sikar	-75000.00		Generator	696688.00	
Satyam Private ITI	100786.00		Green Board	26400.00	
Styam Institute Of Technology	-2196910.49		Invertor	15000.00	
Vedant Institute of Technology	-1965462.00		Lab Equipment	11054151.56	
Vedant Kids	2083847.00		LED TV	24000.00	
Vedant Private ITI	-3366976.98		Misc Fixed Assets	2380111.63	
Vedant Public School	-1020033.22		Mobile	7000.00	
			School Jhula	109000.00	
			Solar Equipment	10725374.00	
			Submersibal Pump	47000.00	
			Ups	1083989.17	
			Vehicle	4738010.71	
			Wall Fan	13220.32	
			Water Cooler	65604.00	

Contd....pg-2

Liabilities	Amount (Rs.)	Amount (Rs.)	Assets	Amount (Rs.)	Amount (Rs.)

INVESTMENTS		**2409723.00**
Accured Int. on HDFC 33930	211,640.00	
Accured Int. on PNB 2869	46,478.00	
Accured Int. on PNB 2948	163,803.00	
FDR with HDFC 133930	1387401.00	
FDR with PNB 2869	157370.00	
FDR with PNB 2948	443031.00	
CURRENT ASSETS		**21972689.6**
Duties & taxes	670844.70	
Deposits Assets	56437.00	
Loan and Advances	21087454.93	
Sundry Debtors	70560.00	
Cash in Hand	644.37	
Bank Account	53531.02	
TDS FY 22-23	14014.00	
TDS FY 23-24	9187.00	
TDS Recivable 15-16	58.58	
TDS Recivable 17-18	9958.00	
177235446.68		**177235446.68**

-

As per our Report of ev
date
For Poonia & Soni
Chartered Accountants

For Vedant College of Engineering & Technology
(Unit: Sanwaria Public School Samiti)

POONIA & SONI JAIPUR CHARTERED ACCOUNTANTS

(CA R. S. Poonia)
#REF!
M. No. 076446

#REF!
#REF!

Date:30/9/2024
Place: Jaipur

Audit Statement

Annexure-12

(A Unit of Sanwaria Public School Samiti)

INCOME AND EXPENDITURE ACCOUNT

(For the Year Ended as on 31st March, 2024)

	Expenditure	Amount (Rs.)		Income	Amount (Rs.)
To	Advertisement Exp.	170000.00	By	Interest on Bank Account	2610.00
To	Affileation (BTER) Exp	37200.00	By	Interest Bank on FDR	96714.00
To	Aicte expenses	370000.00	By	Other Income	50789.00
To	Bank Charges	24784.40	By	Tuition Fee	1331200.00
To	BTER NOC Fees	34000.00	By	TC	2600.00
To	Bus Exp	56434.00	By	Interest on IT Refund	4767.00
To	Conveyance Charges	34170.00			
To	Electricity exp	304558.00			
To	Insurance Charges Loan 5004	2155.00			
To	Int On Loan 5004	915828.00			
To	Interest on HDFCLoan	1431751.00			
To	Internet Expenses	10000.00			
To	Library exp	1040.00			
To	MESS expenses	41028			
To	Miscellaneous Exp.	38519.74			
To	Other Expenses	14220.00			
To	Postage & Courier	879.00			
To	Printing and Stationery	35025.00			
To	Repair and Maintanance Exp.	116434.00			
To	RTU exp	39453.24			
To	Salaries	1210015.00			
To	Scholarships Exp	2000.00			
To	Stationery Exp	1410.00			
To	Travelling Exp.	2040.00			
To	Vechicle insurance Exp.	51035.00			
		-			
	Excess of Income over Exp. (Transferred to Corpus Fund)	**3455299.38**			
		1488680.00			**1488680.00**

For Vedant College of Engineering & Technology

(Unit: Sanwaria Public School Samiti)

#REF!

#REF!

Date:30/9/2024

Place: Jaipur

As per our Report of even date

For Poonia & Soni

Chartered Accountants

(CA R. S. Poonia)

#REF!

M. No. 076446

Annexure-12

Industrial Readiness with Career Planning

The context:

Vedant College of Engineering and Technology objective is not just to help its students to secure a degree but also prepare the students with readiness to face any challenge in their life at any time. We believe that the number of years spent by the students on its campus is extremely impactful as that period witnesses their transformation from scholar to an entrepreneur, executives and successful technocrats. With a deep understanding of students and faculty mindsets gleaned over two decades, the college has formulated list of practices within the Time Table to promote a culture of competitiveness and achieve laurels in their career.

The Practices:

Psychometric Analysis: For the students we conduct psychometric analysis by our certified Professional Mr. Sandeep Meel. First the students are asked to give test having some questionsto test their psychological level then their results are assessed. From this analysis we come to know their problem areas and their interest. After this we take their personnel interviews as a result of which we find out the strengths and weakness of each student and their interests and also their mental level. According to this all analysis, we plan for their future as to what extra-curricular and co-curricular activities need to be performed, do we require communication skill or language class for them, what should be the contents of their personality development programs as per their need and interest. Behind all this our focus is the all round development of our students and help them to attain their goal in life, by providing them the education and skills so that they can excel in their life.

Communication skill enhancement: All the first year students are attached to student counselors. These mentors apart from academic counseling they also help the students to break their inhibitions to face extracurricular events and exhibit their talents with confidence. The skill enhancement includes memory games, tongue twisters and basic grammar using the play game methods etc. Also listening to audio and video clippings will serve the dual purpose of motivating them and teaching them language.

The language lab and soft skill course, which is specifically in English has a diagnostic test, where the tasks and questions are taken from workplace situations is being conducted and students are categorized in to four areas: listening, speaking, reading and writing. This develops, the competencies needed for current and future needs

Interpersonal skills development activities: For the second year students the focus is on

developing soft skills to develop their efficacy in handling situations. The focus for the third year and final year students is on employability skills. They are trained in developing a positive attitude, team skills, adaptability, negotiation skills, critical thinking and personality development. Thus, all these activities help in making students more employable and competitive in the global market.

Technical Training / Certifications: To keep in pace with the latest technologies pertaining to students desire and inclination, a technical value added course is organized for all the Second and Third year students. The course bridges the perceived technical competency gaps between academics and industry. The credentials gained through these courses are very helpful in placement and shows their preparedness to take up the challenge ahead. Certification Course provides a platform as well as resources to help students understand the recent advancements in various fields, which help them refresh & enhance their knowledge base.

Student Workshops: Our College organizes workshops on current technologies in association with reputed industries as well as with MOUs organizations to impart necessary skills for best transition from an Engineering student to an Engineering Professional. These workshops enhance the theoretical concepts learnt by students with hands on practical sessions as well provides an outline for many emerging technologies that are not covered in the syllabus.

Live Projects: Live projects for engineering students gives an edge over the race of recruitment to work hard to ensure a good career. More than the employment practices in recent times students are progressively taking up live projects to pad up their skill set. In spite of practical concepts that one acquire, various industries also need to know students capacity to complete projects using their specific initiative. Hence, we recommend students to do short term live engineering projects during their four years of engineering.

Project Review Process: The best way to master a subject is by doing projects. Through the project, the students not only get a deeper understanding of the subject but also gain hands on practical experience. We insist our students to choose the final semester project title in their area of interest from Smart India Hackathon (Initiative of Government of India) and other social issue related with the real time scenerio in the third year itself. Based on their domain of interest, we allot team members and internal supervisors to each of the project batches and pave way for them to develop their practical and entrepreneurial skill. After title selection, the panel members conduct zeroth review for the students to check the feasibility of their project idea, relevance and applications.

Technical Competitions: Technical competitions are where young brains get to showcase their skills and compete with others to find the best. Such inspiring events that happen in various colleges will guide engineers to dream bigger and make them realised. To provide this great platform, our college grants *On- duty permissions* to all the students who desire to add colours to their resume. The prize winners of college level *'Intra department symposium'* are encouraged and given priority to participate in the technical competitions in other colleges. A technical paper screening committee consisting of peer staff members is established at all departmental levels to guide the students to submit papers for symposiums. Our Chairman periodically meets and encourages these winners for their achievements. The event registration fees, travelling and food expenses are reimbursement to the winners who bag the title of the events. The deserving winners are brought to *limelight* by publicity through daily newspapers and mediaTVchannels. This makes the young minds highly

motivated to do better achievements year by year.

Pre-Placement Activities:

Weekly Online Aptitude Assessments: As we understand that the assessments are a vital part in improving the students'Aptitude skills. We offer the students an Interactive, learning-centric, user-friendly, robust test taking platform which gives immediate, insightful performance report with detailed explanation under CRT PROGRAM.

Quantitative Aptitude Programme: Ability to apply basic concepts of mathematics coupled with analytical reasoning skills to problem solving.

Aspiring Mind's Computer Adaptive Test (AMCAT): This a computer adaptive test ensures the student's proficiency on critical areas like communication skills, logical reasoning, quantitative skills and job specific domain skills.

Co-cubes Pre Assessment Test: It is an online test which measures the student's proficiency on critical areas like communication skills, logical reasoning, quantitative skills and job specific domain skills. Students will get many opportunities to attend campus interview based on their Pre- assess score itself

Mock Interviews: An opportunity to practice one's interviewing skills in an environment similar to an actual interview and to become familiar with interview questions and interview etiquette.

Coding Portal: Students are encouraged to register on online coding portal where students can practice and up skill the student's technical competency.

Evidence of Success:

Since last five years that we had implemented these student support activities, the outcomes of these measures are significant in terms of good number pass percentage, Good Placement records, and student Innovative projects awards and success in technical competitions etc. The evidence of success also could be measured through the publication of scientific research papers, which helped them to get R&D jobs, MS and PhD admission with scholarship in prestigious universities. Success stories are uploaded on our college website that has information about Student achievements and Innovations.

Problems encountered and Resources Required:

Even though, we have highly celebrated practices across in our campus, still it encounters some inherent bottle necks which are well optimized and managed with our expertise.

The constant urge of the student community towards co-curricular training and competitive performances leads to marginal focus destruction from curricular study. Hence for the students, who availed 'On duty' permissions, are provided opportunity to attend extra / remedial classes, so as to improve their marks in theory and practical courses.

To make the skill based training system more effective: training needs to be imparted to faculty members on both design processing and technical skills. Necessary steps are being taken to address this issue

“Outstanding” is what the students rate our efforts of nurturing versatile in all round development. In ACEIT, the management and the faculty members strive to go beyond teaching in an effort to redefine co- scholastic excellence.